

# Programmable Current Mirrors: Design and Applications

by

Sofian Mostafa Abed

A Thesis Presented to the

FACULTY OF THE COLLEGE OF GRADUATE STUDIES

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DHAHRAN, SAUDI ARABIA

In Partial Fulfillment of the  
Requirements for the Degree of

**MASTER OF SCIENCE**

In

**ELECTRICAL ENGINEERING**

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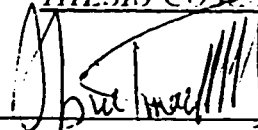
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This thesis written by *SOFLAN MOSTAFA ABED* under the direction of his Thesis Advisor and approved by his Thesis Committee, has been presented to and accepted by the Dean of the College of Graduate Studies, in partial fulfillment of the requirements for the degree of MASTER of SCIENCE in ELECTRICAL ENGINEERING.

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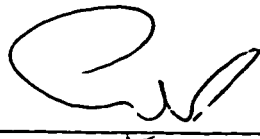
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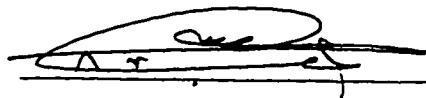
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**To my parents, who learned me how to give**

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## Abstract

**Name:** Sofian Mostafa Abed  
**Title:** Programmable Gain Current Mirrors; Design and Applications  
**Major Field:** Electrical Engineering  
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Current-mode circuits are receiving a great attention nowadays. This is mainly due to their ability to perform well at high frequencies. The work in this thesis deals with current mode circuits. Specifically, a new circuit called multiple output programmable current mirror, PGCM, is constructed. The use of such a circuit in a number of linear and nonlinear applications is considered and discussed in details. Simulation results are presented whenever possible. In most cases, these are in very good agreement with theoretical expectations. Finally, a conclusion is provided together with recommendations for future work.

**Master of Science Degree**  
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**Dhahran, Saudi Arabia**  
**December 1996**

## خلاصة الرسالة

اسم الطالب: سفيان مصطفى عابد.

عنوان الرسالة: مرايا التيار المبرجة ذات المخارج المتعددة: تصميمها وتطبيقاتها.

التخصص: هندسة كهربائية.

تاريخ الشهادة: ديسمبر ١٩٩٦م.

لقد لقيت الدوائر الإلكترونية التي تعالج التيار الكهربائي اهتماما بالغاً في الآونة الأخيرة. السبب الرئيسي هو قدرتها على القيام بأداء فعال حتى عند الترددات العالية. من هذا المنطلق فإن جميع الدوائر المقدمة في هذه الرسالة هي من هذا النوع. في البداية سوف يتم شرح طريقة بناء دائرة جديده تعرف بمرآة التيار المبرجة ذات المخارج المتعددة. يلي ذلك استعراض للتطبيقات المختلفة لهذه الدائرة سواء في مجال الدوائر الخطية أو غير الخطية. بالإضافة إلى ذلك فإن جميع النتائج التي تم الحصول عليها بطريقة المحاكاة سوف تضاف. وأخيراً تقدم خاتمة هذا البحث وبعض التوصايا فيما يتعلق بالمواضيع التي يمكن تطوير البحث فيها مستقبلاً.

درجة الماجستير في العلوم

جامعة الملك فهد للبترول والمعادن

الظهران - المملكة العربية السعودية

ديسمبر ١٩٩٦م



## CHAPTER 1

# INTRODUCTION AND LITERATURE SURVEY

### 1.1 INTRODUCTION

In the past, analog signal processing techniques were characterized by their complexity, large area and by the difficulty of integrating analog systems in a single silicon chip. With the current advances in VLSI technology in addition to the evolution of new analog signal processing techniques, these problems started dissolving. Nowadays, very small transistor areas are being achieved specially for MOSFETs. Also, the performance of PNP transistors has become compatible with that of the NPN in BJT transistors. In addition, new techniques like, current mode and switched current circuits, switched capacitors, active R, OTA-C, the translinear principle and more recently log domain

filtering are being extensively utilized. All these factors resulted in increasing the research efforts and in opening new search areas in the field of analog signal processing. Nowadays it is well agreed that analog circuits constitute a potential trend in the implementation of electronic systems in the next century.

In analog signal processing, the research is directed mainly in the three directions. Some researchers are involved in transistor level based systems while others are concerned with applying the available building blocks to build their required systems. In contrast to digital systems, analog building blocks are not always readily available. For this reason some research is directed towards implementing new analog blocks starting from transistor level. Throughout these directions, transistor based designs seem to be the most complicated. However, they provide superior advantages over the others. They lead to circuits with very efficient utilization of the chip area and power consumption. Power consumption is becoming an important issue for the circuits of the next century. Also, in some techniques like log domain filtering and translinear circuits, they exhibit very excellent bandwidths. In addition, they constitute the base for the developments of the available ,or new, analog blocks.

The work in this thesis is oriented to the design of new current mode analog signal processing circuits. Transistor based designs are used to implement linear and nonlinear circuits. Hopefully this will result in an increase of the library of analog signal processing cells. In the linear part, a new multiple output electronically programmable current

conveyor will be introduced. This new block will be used to implement a universal filter and oscillator circuit. In the nonlinear part, analog computational circuits will be developed. These include circuits that perform two quadrant multiplication, one over circuit, exponentiating circuits, programmable analog function synthesizing circuits and finally circuits for frequency multiplication. In all these circuits, the current mode approach is emphasized mainly because of its excellent bandwidth. Basically all designs make use of a recently published circuit of an electronically programmable current mirror, see [1]. The wide versatility of the unity gain current mirror was the main motivation for investigating new applications of this new circuit.

## 1.2 LITERATURE SURVEY

In this section, a quick review of previous related publications will be presented. The survey is divided into two parts. First an overview of recent developments in the implementation of current conveyors, CCIIs, will be given. Then, in the other part, nonlinear circuits built from available building blocks or transistor level based circuits will be discussed. Throughout this survey, a comparison between each work with its other related works will be made and the things that have not yet been achieved will be pointed out.

## 1.2.1 CURRENT MODE CIRCUITS

**1.2.1.1- Current Conveyor Implementations** Since the development of the first generation current conveyor, CCI, by Sedra and Smith in 1968 [2], many trials have been done to make new topologies of this circuit to overcome its nonidealities. Also, the second generation current conveyor, CCII, was built in the same period. At the beginning, BJT implementations of both conveyors were done. This is mainly due to the high speed of the BJT circuits compared to its CMOS versions. The CCI proposed first by Sedra uses both NPN and PNP transistors in its implementation. For this reason, it suffers from a small DC offset between its X and Y input terminals. Moreover, because of the finite beta and the early voltage effects, the transfer ratio between the currents  $I_z$  and  $I_x$  is not unity. Finally, the input impedance at terminal X, although small, is temperature dependent.

Another implementation was proposed in 1978. It is based on the power supply current sensing technique, [3]. This technique relies on sensing, using simple current mirrors, the collector currents of the output transistors of the translinear circuit at the output of an Op Amp. This method resulted in reducing the input offset voltage to that of the used Op Amp and reduced the input impedance at X terminal because of the feedback around the Op Amp. Although the amplifier is connected as a buffer, still the bandwidth of the resulting conveyor is smaller than the one obtained by conveyors built from translinear circuits. This type of circuits will be discussed later in this chapter. Only when the

bandwidth of the Op Amp is high, then the conveyor BW will be increased. This means more complicated design structures are required for CCII's based on this technique.

Recently, more concentration was given to the power supply current sensing technique. In [4], Lidgey and Su referred the error in the transfer ratio between  $I_x$  and  $I_z$  to the finite output resistance and capacitance of the biasing current source of the translinear circuit at the output of the amplifier which results in nonzero sensed current when terminal X is not connected to any load. They suggested bootstrapping the power supply, both positive and negative, of the current conveyor, by the input common mode voltage. This makes the voltage at this output impedance almost equal to zero. Also, the Early voltage effect is eliminated. These variations result in improving the transfer ratio of  $V_x / V_y$  and  $I_z / I_x$ . Experimentally, significant improvements in both current and voltage transfer accuracy were attained.

Toumauzou and Lidgey, published a detailed analysis of IC Op-Amp power-supply current sensing in 1994, [5]. In this work, closed form expressions for both sensed currents were given. Based on this, it was concluded that the PSRR of the Op-Amp has a large effect on the op-amp power supply currents, especially at middle and high frequencies. Also, power supply non-ideal currents increase with frequency and become very large at high frequencies. Based on these results, a new improvement in this technique was suggested. It was shown that by sensing only currents of the output stage

of the op-amp, nonideal sensed currents are reduced to about one third of their previous values.

CMOS realizations of both CCI's and CCII's were suggested. The main motivation for doing so is to provide compatibility with the commonly used MOS technology for digital systems. Although MOSFETs are generally slower than BJT's, they are more accurate. This is because of their negligible gate currents. However, direct translation of BJT conveyors to CMOS technology results in several drawbacks. E. Bruun has provided several topologies for CMOS versions of both conveyors, [6, 7]. He showed how a combination of basic building blocks can result in high speed and high precision CMOS current conveyors, [7]. In a recent work, he suggested the use of partial current feedback from X to Y terminals and constant current biasing of the input transistors of the class AB CMOS current conveyors in order to stabilize the quiescent current of the input stage, [6]. This will also result in a constant, process independent input impedance.

All these efforts concentrate on characterizing and enhancing the performance of current conveyors. On the other hand, some researchers are trying to modify the basic conveyors structure to obtain better analog blocks. For example, Fabre, see [8], has developed a third generation current conveyor, CCIII. This new conveyor, is described by the same equations characterizing CCI, except that  $I_y = -I_x$ . This feature enables the CCIII to be used in sensing currents that flow in a floating branch of a circuit. It may also be advantageously used as the input cell of probes and current measuring devices.

The design of programmable current conveyors is also attracting a number of researchers. In [9], a new wideband current amplifier and current conveyor were developed. The feedback theorem was used extensively in order to build a programmable gain current mirror. Although gain is programmable, the BW of such a mirror is fixed and wide. Also, a new highly accurate unity gain current mirrors were developed. Moreover, a current buffer with a simple structure and having a wide bandwidth was built. In all these circuits, only NPN transistors were used. With a load of 100 Ohms, the 3db bandwidth of such a circuit was 90 MHz. A disadvantage of this circuit is that it does not provide high gains. The same strategy was followed by Fabre and Mismeche in 1994, see [10]. However, the programmable current mirror obtained in [10] is based on the translinear principle. Unfortunately, the BW of this circuit is not more than 100 KHz . Also, since the translinear cell is used for sensing the input current, the input impedance is not very small and is temperature dependent.

Another method of designing Programmable CCII's was considered previously in 1988, [11]. In this method, a transistor is used to feed back the output of an Op Amp to its negative terminal. This resulted in equal voltages at the input terminals of the amplifier. The collector current of this transistor is applied as an input to a differential current amplifier which has a programmable gain. The output of the current amplifier is then subtracted from a DC current to make it having no offset. This output is the Z output of the CCII. Experimental results show good accuracy of the output up to a gain of 10. The bandwidth of this conveyor is more than 10MHz. The authors successfully used this

programmable CCII to implement electronically programmable grounded inductors. Also, four electronically tunable negative resistance converters were suggested. However, these circuits utilize more than one conveyor and use a large number of passive components.

**1.2.1.2- Developments in Current Mirrors** Current mirrors are well known for their excellent bandwidth which is independent of gain. They are extensively used in many current mode building blocks. For this reason, they are receiving a great attention. Some researchers focus on calculating and enhancing their high bandwidth, [12,13]. Others follow another approach trying to build programmable current mirrors better than the ones available, [14-18]. Programmable current mirrors are often used to build new programmable current conveyors or amplifiers. In this short survey, examples on both approaches will be given.

An example of the first approach, concerned with enhancing the BW, is a recent work done by Vou and Toumazou, [13]. In this paper, they suggested a new high speed current mirror compensation technique. Using analytical calculations, they found that the BW of the simple current mirror is equal to half the cutoff frequency of the transistors used in it. By adding a resistance, equal to the input resistance of the transistor used at the input of the mirror, the BW doubles and becomes equal to the cutoff frequency.

Another example for BW improvement of CMOS cascode current mirrors, is found in [12]. Cascode current mirrors are usually utilized whenever current mirrors with high output impedance and low static error is required. However, this solution leads to a decrease in the high frequency performance compared to the simple current mirror.



To gain advantages of both the simple and cascode current mirrors, classical improved cascode current mirrors are used. The problem of such a circuit is that it leads to instability problems without an easy way to find the boundary conditions. The proposed circuit in [12] achieves both higher high frequency performance and lower static error and does not have any instability problems. With respect to traditional cascode current mirrors, two transistors are added in this new circuit. The first has the purpose of pumping current in the gate- source capacitance of the lower two transistors. The second, which is diode connected, realizes a low- impedance route to ground for the source current of the previous added transistor. With this method and using analytical calculations, the obtained BW is similar to that of the simple two transistor current mirror which is equal to half the cutoff frequency of the transistor. The proposed circuit was built in 2  $\mu\text{m}$  technology and simulation results agree well with theoretical results.

The second approach, concerned with programmable current mirrors, was pointed previously when programmable conveyors of Sedra, Smith and of Fabre were considered. In another paper [14], whose author received a patent for it, a high ratio wide range controllable current mirror was designed. The circuit, composed of only three transistors, can be used as a current amplifier with constant bandwidth too. Basically, a grounded resistor is added to the emitter of the input transistor of a simple current mirror. A DC current source pumps current into this resistance and produces a constant DC voltage across this resistance. This voltage causes a nonlinear gain between input and output

currents, as can be seen from the translinear principle. Thus a high gain is obtained while the bandwidth of the mirror is not affected.

CMOS programmable current mirrors were also considered by some authors, [16, 17]. In [16], two programmable CMOS current mirrors were proposed, one for differential inputs and the other for single-ended inputs. The principle of operation relies on obtaining the sum and the difference of the input current and a control current. The two currents are then converted to two voltages applied to two identical transistors operating in saturation. By making use of the square law characteristics of MOS transistors operating in saturation region, the resulting differential current at the drains of the two transistors becomes a linearly amplified version of the input current. The gain is controllable via the DC control current at the first stage of the circuit. Using this method, gains up to several hundreds are obtainable without affecting the BW of the cell. The maximum gain bandwidth product obtained was 185 MHz. A major problem of this kind of circuits is the limited bandwidth which is due to the nature of MOS transistors. For this circuit, the BW was about 1 MHz only.

### **1.2.2 Nonlinear circuits and systems**

Nonlinear circuits constitute an important part of analog circuits which is rapidly growing. This is mainly due to the development of the translinear principle for both BJTs

and MOSFETs and of new analog signal processing tools. In this section, an overview of the design strategies of nonlinear circuits will be given. These designs are divided into three categories. In one class, transistor based designs are introduced while in the other, designs based on available building blocks will be presented. Finally, a special section is devoted for the different topologies of analog multipliers and dividers.

**1.2.2.1 Transistor-Level Based Circuits** One of the oldest methods used to design function generators is the linear segment approximation technique. This technique is based on obtaining a transfer function with linear segments connecting a large number of breakpoints in order to convert a triangular input signal to a sinusoidal one or any other desired shape. The resulting transfer function becomes nonlinear if the number of breakpoints is sufficiently large. At the beginning, these points were selected randomly, see [19]. In [20], the design was based on given breakpoints, while in [21] a simple formula for calculating these points was introduced. Schiffer and Evans, [22], designed a tri-wave to sine shaper that reduces the deficiencies of peak and crossover distortion compared to previously reported methods.

In the late 1960's, a new powerful technique for implementing nonlinear circuits started emerging. This technique is called the translinear principle. In 1968, Gilbert, [23], introduced the first wideband amplifier based on this principle. Later, the same principle gained a widespread use in circuits like multipliers, dividers, squarers, high-power function generation, r.m.s. converters, vector magnitude generators, geometry-correction

systems for c.r.t. displays etc. It was also used to obtain very wideband linear amplification, analog signal normalization, sine / cosine synthesis and many other special algebraic functions. Nowadays, many transistor based nonlinear circuits are designed using the translinear principle. A proposed classification of translinear circuits was given by the same author in 1975, [24], where he redefined this principle in a new versatile form and proved it mathematically for BJT transistors.

Later, in 1991, Seevinck and Wiegink succeeded in generalizing this principle to include both BJT and MOSFET transistors, [25]. In this paper, the MOS translinear circuit principle was derived and an initial classification of simple MOS translinear circuits was proposed. A previous work of Seevinck was to formulate a step by step procedure to obtain approximations of trigonometric functions and their inverses. The approximations are simple, in the sense of containing few terms and having numerical coefficients with three or less significant figures, and are valid over a wide interval. The absolute error of the developed approximations is less than 0.25% of maximum. These approximate expressions were derived mainly to be synthesized using the translinear principle. The paper contains an example of such a translinear circuit for the cosine function.

The most recent development in this principle was the application of the back gate in MOS weak inversion transistor circuits. In this paper, [26], the four terminal point of view is elaborated with respect to MOS weak inversion translinear circuits, a class of circuits naturally very suitable for low-voltage and low-power applications. It is shown

how the use of the bulk terminal as a second gate enables us to design translinear circuits that are not possible when using bipolar transistors.

Another class of accurate nonlinear circuits that are transistor based relies on the square-law characteristics of MOS transistors. A good example of this kind of circuits is given in [27]. Using a two-transistor circuit having a constant sum of their gate source voltages, expressions are derived for the sum and difference of drain currents. Based on these relations, six circuits were derived. These include linear  $I - V$  and  $V - I$  converters, current squaring circuits, divider and multiplier circuits and finally a current inverter. More elaborate circuits were then built using these functional blocks.

Finally, a recent trial, [28], was made to integrate various analog computational circuits to form functional blocks that are integrated in a generic analog processor. The operation of the processor can be programmed by digital control signals. Furthermore, it provides serial outputs as well as parallel outputs, and can be expanded to a larger system by connecting the serial ports of the chip set together. The processor architecture is flexible and modular to accommodate different system architectures for image signal processing applications. For the neural net applications, the processor can be used as a coprocessor with a conventional digital computer to speed up the simulations of a variety of neural network algorithms.

**1.2.2.2 Designs Based on Available Building Blocks** An alternative approach for designing nonlinear circuits and systems is to make use of available building blocks. These include multipliers, operational amplifiers, transconductance amplifiers, current mirrors,

and current conveyors. Gilbert used his novel analog multiplier to implement several powerful function synthesis circuits, [29]. These functions include two-variable four-quadrant multiplication, two-variable two-quadrant division, one-variable two-quadrant squaring and one-variable one-quadrant square-rooting. Moreover, other complicated functions like  $X^n$  for any  $n$  from 0.2 to 5, the percentage difference between two quantities, approximation of sine, cosine, and tan functions, absolute-value of a variable, odd-order squaring and square root of a signal with unknown polarity, were built using one multiplier chip, the AD534. With two multipliers, very accurate (theoretically 0.009% error) two-quadrant synthesis of  $\sin$ ,  $\tan$ , and inverse trigonometric functions, two-dimensional vector sum, vector rotation and resolution, and four-quadrant division, was achieved. Furthermore, frequency multiplying circuits were also obtained. The main disadvantage of all these designs is the bulky area required by each design because the AD534 itself contains three differential amplifiers in addition to one multiplier and one reference and biasing circuit.

Operational transconductance amplifiers, OTAs, can also be used for nonlinear function synthesis. The OTA's programmability nature and the fact that OTAs have only a single high impedance node, in contrast to conventional op-amps make the OTA an excellent device candidate for high frequency and voltage (or current) programmable analog basic building blocks [30]. Using two OTAs, for negative and positive inputs, a four quadrant voltage multiplier can be made if the transconductance is varied through

one of the multiplied signals. A divider can also be implemented if feedback is used with an OTA multiplier. By connecting the output of a single OTA to the previous multiplier and connecting the final output to both inputs of the multiplier, a square root circuit is obtained. Moreover, exponentiation operation can be synthesized if the same input voltage is applied to more than one multiplier and some OTAs are connected as loading resistors to convert output currents of these multipliers to input voltages for other stages. Using these relatively simple blocks, more complicated rational expressions can be synthesized.

Another method of synthesizing nonlinear characteristics is the piecewise linear approximation technique, [30]. A one segment piecewise linear curve can be synthesized with only one OTA having one of its input terminals connected to a reference voltage and a diode connected at its output. The slope of such a segment is controllable via the control of the OTA transconductance. The number of linear segments required to approximate a nonlinear function is equal to the number of OTAs to be used in this method.

Although the use of OTAs provides the feature of programmability of the obtained transfer functions, it suffers from many serious problems. The first is the fact that the  $V$ - $I$  characteristics of OTAs themselves are temperature sensitive. Also they suffer from a limited input dynamic range and a considerable input offset. Furthermore using OTAs as building blocks results in extensive area consumption by the required nonlinear systems

specially for realizing practical functions like the sin function for example. On the other hand these devices enjoy very good frequency characteristics.

Another nonlinear application for OTAs was considered recently in 1993, [31]. In this paper, the use of OTAs was suggested for performing exponentiation operation. The exponent, which is a fixed integer or a rational number, is determined by the number of OTAs to be used. The main idea is that the control signal, used for adjusting the transconductance, is made proportional to the input voltage using another OTA. The same thing is repeated for every added OTA until the required degree of exponentiation is obtained. The final output current is entered through another OTA connected as a load in order to convert this current into a voltage. For rational exponents, this voltage is applied again to several number of OTAs, according to the desired exponent, in the same manner of connecting the input voltage. Finally, the output voltage is set equal to the input voltage raised to a power of  $M/N$  where  $M$  and  $N$  are determined by the number of OTAs used in both branches of the circuit.

Although this technique is very powerful and results obtained experimentally exhibit a very good accuracy, still the previously mentioned drawbacks of using OTAs are valid. Moreover, the technique fails when the desired exponent is relatively large. Furthermore, the value of the exponent is fixed and is not easily programmable nor is allowed to be time- varying. In order to reduce the exponent by one, four OTAs need to be canceled. Much simpler methods with less area consumption are required in order to make the



exponentiation circuit more suitable to be used in other electronic systems. This will be the subject of this thesis in chapter 4.

MOS transistors operating in their triode region together with current conveyors, CCII's, or usual operational amplifiers were used also to synthesize four-quadrant multipliers and two-quadrant dividers in addition to some other nonlinear functions, [32, 33]. These designs rely mainly on the nonlinear equations of MOS transistors in this region of operation. CCII's were considered to design piecewise linear functions too. The idea is very similar to that of OTAs. A new very attractive feature offered by the proposed circuit in [32], by Ismail and Khashab, is the ability to process multi-inputs with only one circuit. In addition, the proposed circuit is configurable to perform multiplication or division. Other suggested applications of the circuit is square rooting, scalar vector multiplication and obtaining the inverse of a weighted sum. Also, they proposed a circuit for implementation of the synaptic weights of a feedback neural network. The circuit is simple, versatile, its output voltage is programmable and it offers an economical way for the silicon implementation of such networks.

To eliminate the need for complex structured OTAs, a new methodology for piecewise-linear approximation using current mode circuits with very simple topologies was first issued in 1992, [34]. Four basic building blocks were suggested for this technique. Each block generates a transfer function with one linear segment and one breakpoint. The position of this breakpoint is varied to all four quadrants throughout the four blocks. Also, the slope of the segment is positive in two of these blocks and negative

in the other two. This slope is determined by the ratio of transistor areas in the case of unity gain current mirrors, or by the gain in programmable gain current mirrors. Different combinations of these blocks can yield many nonlinear functions.

**1.2.2.3 Designs of Multipliers and Dividers** Designing analog circuits to perform an accurate 'one-over' function is difficult. Traditional approaches use multipliers in feedback circuits [32,30]. However, VLSI implementations of these circuits is challenging. On the other hand, a new simple but highly linear CMOS circuit to compute this function was proposed in 1993, [35]. The idea is based on utilization of the natural inverse relationship between the resistance of CMOS transistors, operating in the linear mode, and the gate source voltage. However, this relationship is nonlinear due to its dependence on the drain-source voltage. According to the author, the main source of nonlinearity is the mobility degradation and not the higher order terms of the drain source voltage. Hence, the nonlinearity appears as a constant which can be easily canceled. Such a circuit does not require high degrees of component matching because of the offset cancellation technique that is used at the output stage.

The translinear principle can also be used to implement analog dividers. For example, a simple low voltage weak inversion MOS  $1/x$  circuit has been proposed in [36]. A breadboard realization of this circuit provides an output with an accuracy of +4% / -8% with respect to the desired transfer characteristics over an input current ranging from 6 pA to 2nA. This circuit is suitable for low power applications. It operates at a supply

voltage that is a few hundred millivolts above the threshold voltage. Similarly, a number of techniques can be followed to implement four quadrant multipliers.

Gilbert introduced his novel multiplier in the late 60's, [23]. This bipolar multiplier has the capability of multiplying two signals with a high accuracy and fast response, even with large inputs (  $20\text{-}V_{pp}$  ). It is based on the variable transconductance scheme which operates on Gilbert's translinear principle. Later, several schemes followed the same methodology to generate other bipolar topologies, [29]. For this class of circuits, the exponential characteristics of the bipolar transistor is used. Namely, by adding voltages in loops involving base emitter junctions, the products of various branch currents are generated. Applying a similar technique for the MOS technology, using the square law characteristics, unfortunately, does not produce such useful results. Hence, more suitable schemes must be sought.

The first MOS version of Gilbert's translinear multiplier was introduced first in 1985, [37]. First, a method for linearizing the source coupled circuit, by adding a current nonlinearly proportional to the input voltage to the tail current, was discussed. This method was extended to linearize the MOS version of Gilbert six transistor multiplier. Then a folded cascode version of the resulting circuit was made in order to increase the differential input range. The resulting circuit exhibits a bandwidth of 1.2 MHz. Over an input voltage ranging from -10 to +10 volts, a nonlinearity of 1.6% and 1.3% of full-scale X and Y inputs respectively, was observed. These nonlinearities are due to deviation from square law characteristics and to device mismatches.

One of the best CMOS multiplier implementations, in terms of simplicity and frequency bandwidth, was proposed in a recent publication, [38]. In this circuit, four MOS transistors together with another four voltage sources connected at their drains are needed. If these MOSFETs are operated in the linear mode, then it can be easily shown that the result of subtracting the sums of the drain currents of every two transistors, alternatively connected to both input voltages, is linearly proportional to the multiplication of the two input signals. Two methods of implementing the four voltage sources were suggested. In one method, only CMOS transistors are used while in the other BJTs are used instead. The BICMOS version of the multiplier was found to have less than 0.1% THD for balanced inputs, even with 2% transistor mismatch, and a bandwidth of 100 MHz in a standard 2  $\mu$  m process. This is considered an excellent achievement.

### **1.3 THESIS OBJECTIVE**

From the preceeding introduction, the main objective of this thesis can be outlined. This work concentrates more on showing the wide versatility and the practical usefulness of bipolar type programmable gain current mirrors. It is the goal of this thesis to explore and examine possible applications of PGCMs. Most of the testing will be done through circuit simulation. However, all devices models, mainly transistors, are obtained from SPICE library. In brief, the main objectives of this thesis are the following :

- Overview of the design strategy of the linear PGCM suggested in [1 ,15 ].
- A number of applications, both linear and nonlinear will be given. For every application to be included, the linear PGCM is modified to suite the desired function being implemented.

- Finally a conclusion is made. This briefly outlines important achievements and answers the question raised at the beginning regarding the usefulness of the PGCMs in analog systems.

## CHAPTER 2

# Linear Applications ;Filters & Oscillators

### 2.1 INTRODUCTION

In the past few years, current mode circuits has attracted a large number of researchers. This is mainly due to their high frequency bandwidth. The most commonly used current mode building block is the second generation current conveyor. A wide range of applications of this block is present in the literature. Simple and powerful implementations of all kinds of filters with minimum number of passive components and highly reduced sensitivities are also available. However, in most of these implementations, independent electronic control of all filter parameters is not provided. Although a number of programmable filters has been presented recently, these circuits require a large number of CCII's and OTA's to obtain full independent electronic control on all filter parameters.

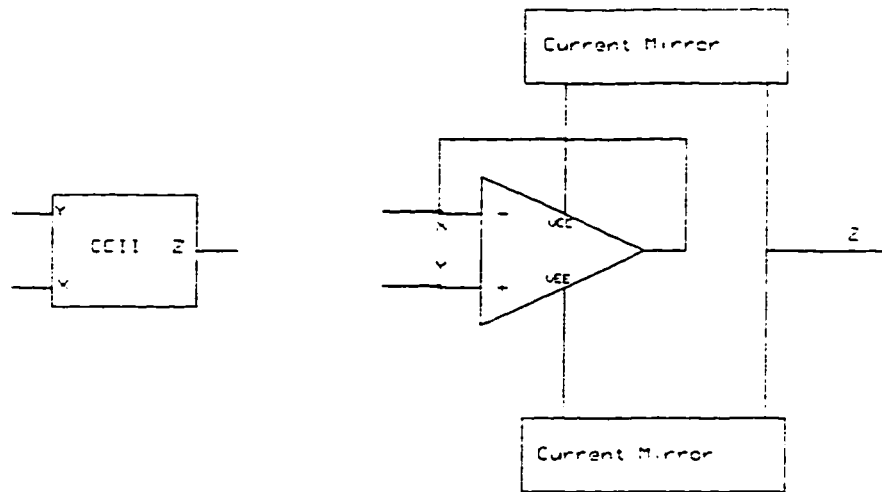
In this chapter, a new block is presented. It is basically a modified version of the second generation current conveyor. It has two additional new features. The first is the availability of more than one output. Secondly, each current is gain programmable independently. It will be called multiple output programmable current conveyor or briefly MOPCC. Such a block is expected to prove itself in applications where full independent electronic control is desired.

The first section of this chapter will introduce an IC design of the MOPCC, and simulation results showing the high frequency performance of the circuit will be shown. In section II, the use of MOPCCs in implementing a programmable universal filter will be explained. It will be shown how the same circuit can provide a programmable oscillator too. Finally, simulation results that support theoretical derivations will be given. This is followed by a brief conclusion.

## 2.2 DESIGN of MULTIPLE OUTPUT PROGRAMMABLE CURRENT MIRRORS

One of the most powerful implementations of the second generation current conveyor is based on power supply current sensing technique [4,39]. This technique is based on sensing current variations in the power supply of an operational amplifier as shown in Figure 2.1.





**Fig 2.1** Power supply current sensing .

Using the same topology, if unity gain single output current mirrors are replaced with multiple output programmable current mirrors, then a MOPCC is obtained. Also, it is desired that these current mirrors be linearly programmable with minimum temperature effect.

To start with, a single output linearly programmable current mirror is designed, then the idea is extended to multiple output PCM's. The first linearly programmable current mirror in bipolar technology appeared in 1992 [15]. It was used to implement a wide range linearly programmable OTA. Recently, a bipolar class AB linearly programmable

current mirror in both bipolar and MOSFET technologies was presented [1 ]. The basic idea is shown in Figure.2.2. From this figure it can be seen that

$$V_{be1} + V_{c1} = V_{be2} + V_{c2} .$$

$$V_T \ln ( I_{in} / I_s ) + V_{c1} = V_T \ln ( I_{out} / I_s ) + V_{c2}$$

$$V_T \ln ( I_{out} / I_{in} ) = V_{c1} - V_{c2}$$

$$\text{Thus Gain} = I_{out} / I_{in} = \text{Exp} [( V_{c1} - V_{c2} ) / V_T]. \quad (2.1)$$

Mainly, the two voltages  $V_{c1}$  and  $V_{c2}$  are used to control the gain of the unipolar mirror. To linearize this gain, these DC voltages must be a logarithmic function of a control variable. Also, to cancel the requirement of zero output resistance of the control voltages, composite bipolar transistors are used. This way, current passing through these resistances becomes negligible and similarly the voltage across them. This completes the design of the unipolar programmable current mirror. Such a mirror is shown in Figure.

2.3. From this figure, it can be seen that

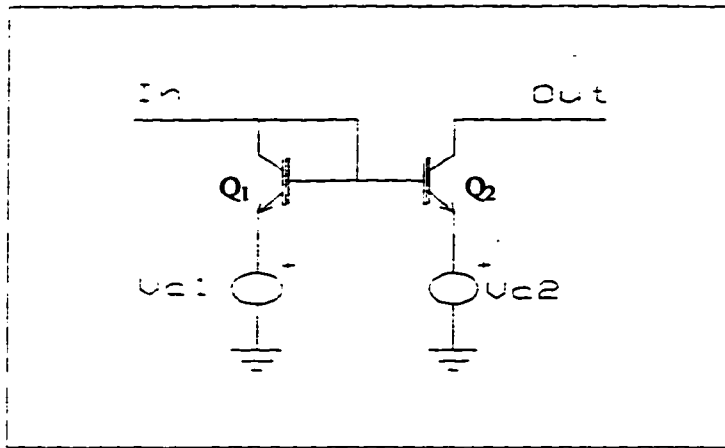
$$V_{c1} = 2V_T \ln ( I_2 / I_s )$$

$$V_{c2} = 2V_T \ln ( I_1 / I_s )$$

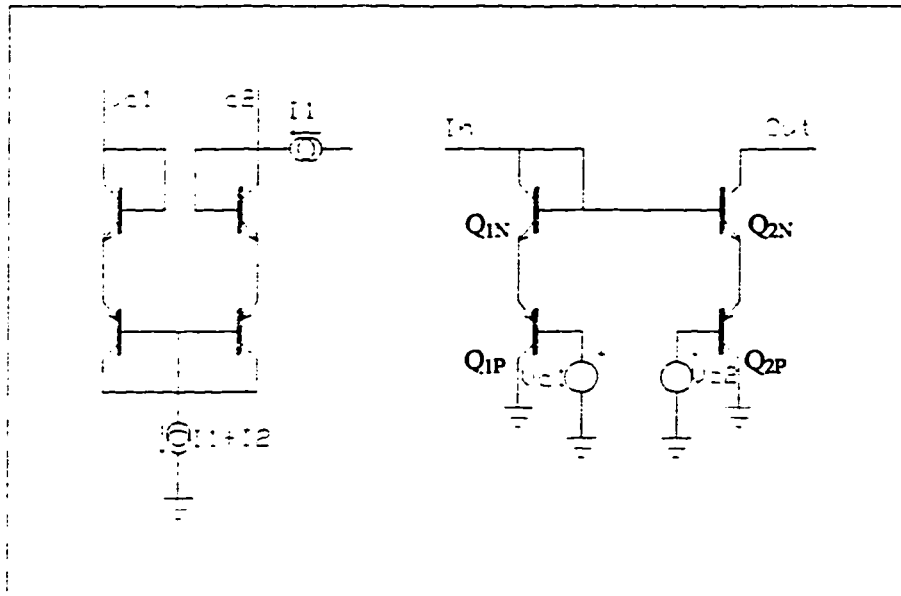
$$\text{Gain} = \text{Exp} [2V_T \ln ( I_2 / I_1 ) / (2V_T)]$$

$$\text{Thus Gain} = I_2 / I_1 . \quad (2.2)$$

Two of these circuits were used in [1] to get the new bipolar programmable current mirror. In this circuit, shown in Figure. 2.4.,  $Q_1$  - $Q_4$  constitute a class AB input stage. This stage has a small input resistance in order to absorb all the input current. In addition, the difference between collector currents of  $Q_1$  and  $Q_3$ , which is equal to  $I_{in}$ , is sensed by the upper and lower current mirrors obtained from  $Q_5$  - $Q_8$  and  $Q_9$  - $Q_{12}$  respectively. Notice that these current mirrors are built from composite bipolar transistors like  $Q_5$  and  $Q_6$ . Transistors  $Q_{13}$  - $Q_{16}$  together with  $I_1$  and  $I_2$  constitute the control circuit for the upper mirror. Similarly, the control circuit for the lower current mirror is composed of transistors  $Q_{17}$  - $Q_{20}$ . Control currents  $I_1$  and  $I_2$  are connected such that  $I_1$  passes through  $Q_{13}$ ,  $Q_{16}$ ,  $Q_{18}$  and  $Q_{19}$  while  $I_2$  passes through the rest of the two control circuits. By making use of this fact, simple mathematical manipulations lead to the same expression in Figure 2.2 for  $V_{c1}$  and  $V_{c2}$ . Notice that, for this expression to be valid, it is assumed that all base currents are negligible. Also,  $I_A$  and  $I_B$  have to be sufficiently large to bias  $Q_2$  and  $Q_4$ . This circuit has a constant bandwidth of 20 MHz and a wide range of programmable gain. However, it can't be used to implement multiple outputs.



**Fig 2.2.** Principle of Gain programming.



**Fig 2.3.** Circuit of control voltages

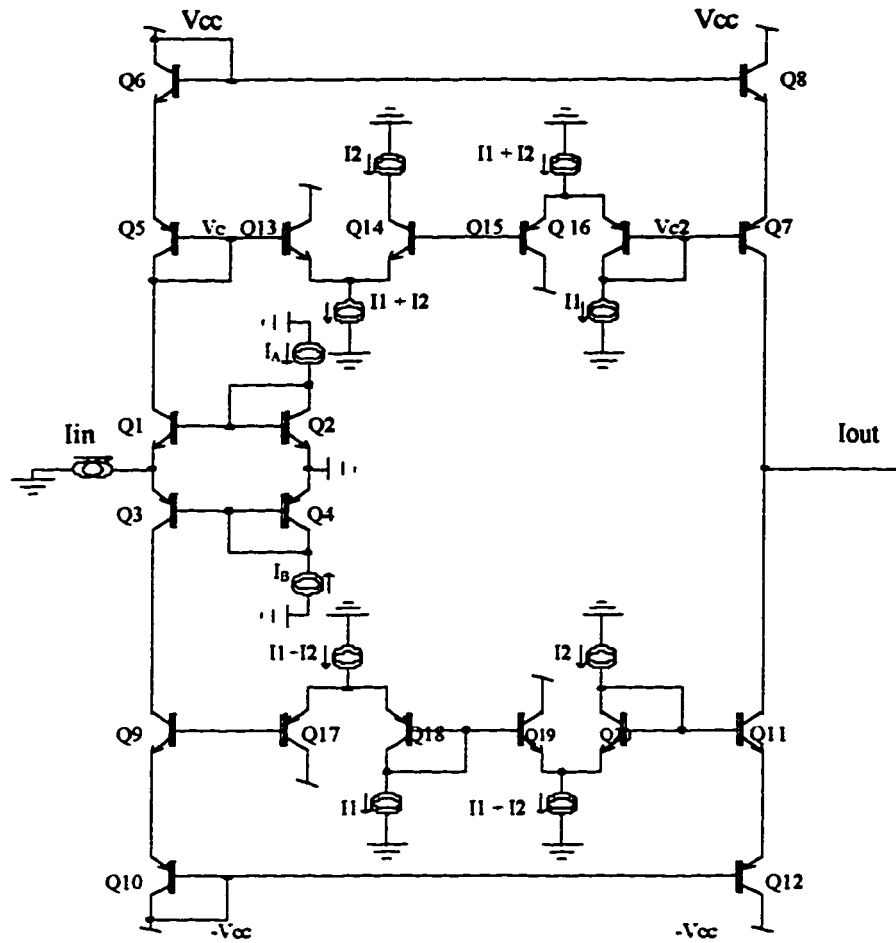


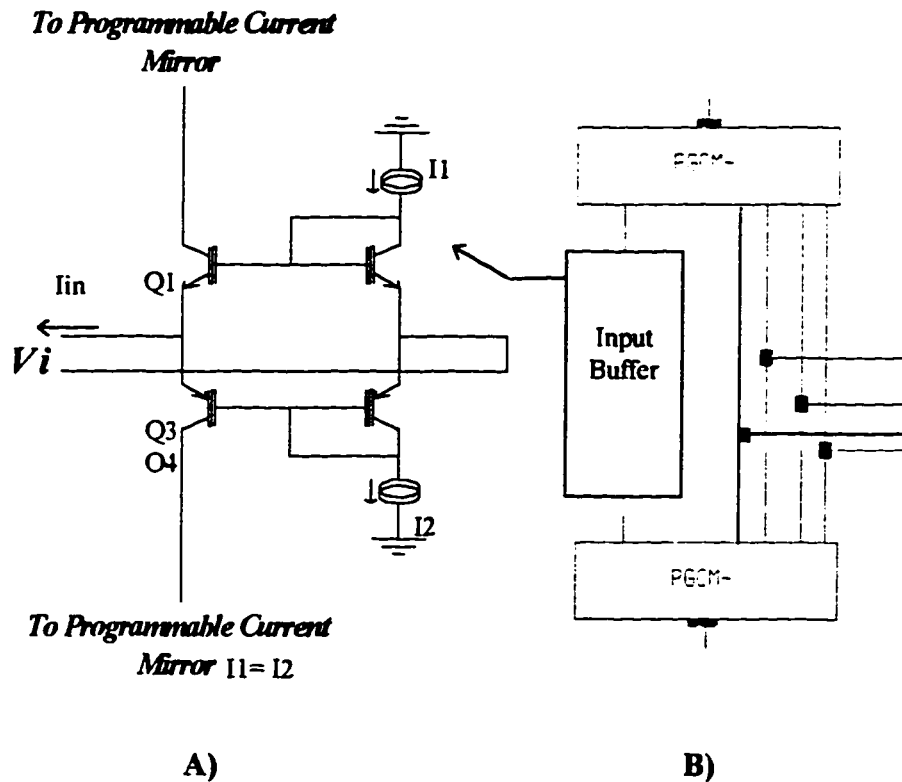
Fig 2.4. Class AB programmable current mirror.

## 2.3 DESIGN OF MULTIPLE OUTPUT PROGRAMMABLE CURRENT CONVEYORS

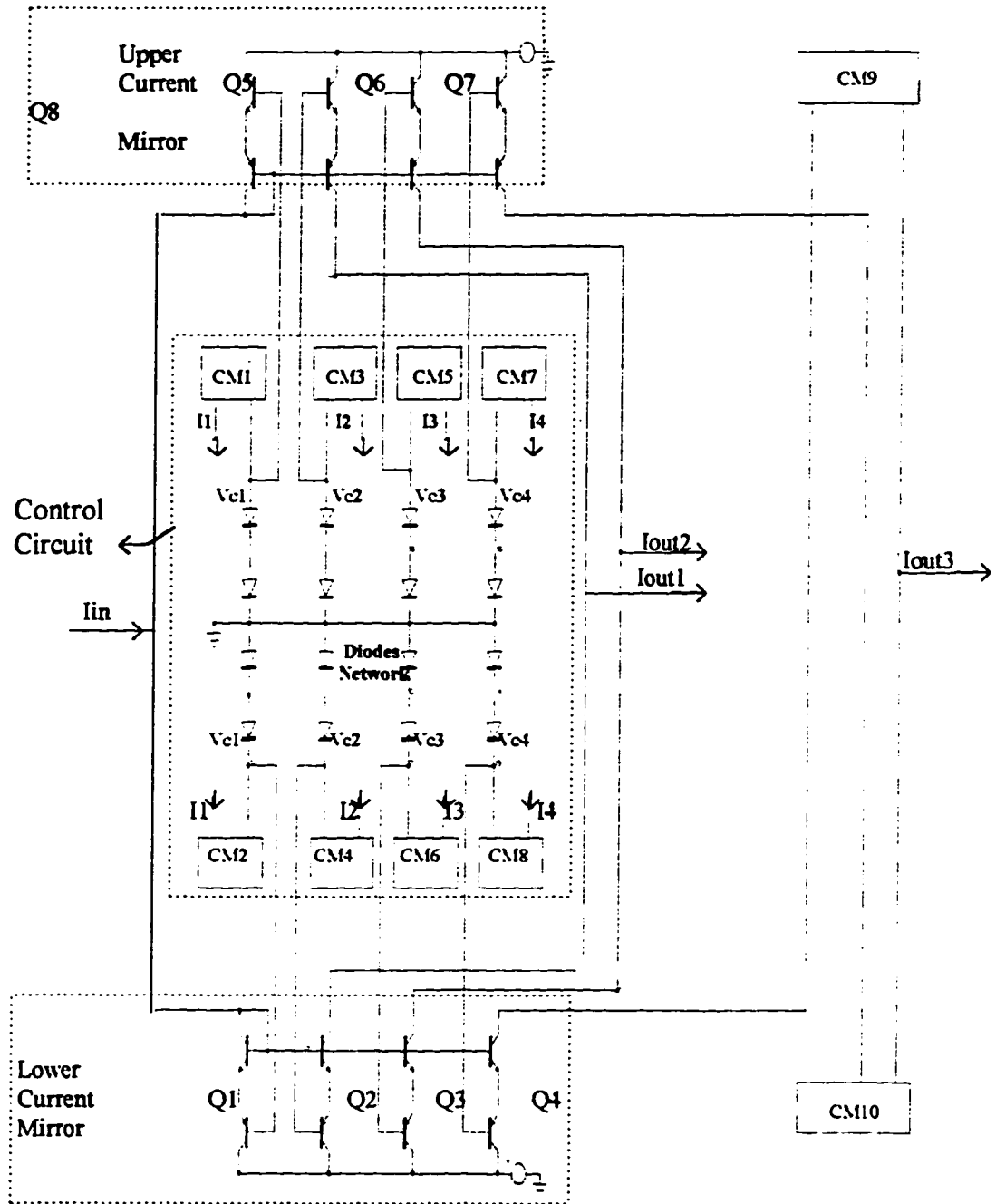
**2.3.1 Design Procedure** Figure 2.5. shows a simplified schematic diagram of the internal circuit of a three output PCC with one of the outputs,  $I_{out3}$ , provided by a negative gain. In this diagram,  $I_1$  -  $I_4$  are control currents used to obtain the control voltages  $V_{c1}$  -  $V_{c4}$  by being fed to the upper part of the diodes network. These control voltages are used to control the gain of the upper current mirror. The expression for these voltages is the same as the one in Figure 2.3 for  $V_{c1}$  and  $V_{c2}$ . Transistors  $Q_5$ -  $Q_8$  form the upper current mirror and are composed of both NPN and PNP transistors combined to build one composite BJT transistor, see Figure.2.3. Thus the control circuit is built from the diodes network plus a number of current mirrors proportional to the number of outputs plus one. The first output is taken from  $Q_6$  and is provided a gain equal to  $I_2 / I_1$ . Notice that the upper current mirror is an extension of the one in Figure 2.3. It is extended to have three output with each output being controlled by a different control voltage,  $V_{CN}$ , where  $n = 2, 3$  and 4. Similarly the diodes network is an extension of the one in Figure.2.3. The same description is valid for the lower current mirror being controlled by  $I_1$  -  $I_4$  which produce control voltages  $-V_{c1}$ ,  $-V_{c2}$ ,  $-V_{c3}$ , and  $-V_{c4}$ . By adding outputs from upper and lower current mirrors, a bipolar programmable current mirror is obtained. The gain for output one is  $I_2 / I_1$ , for output 2 is  $I_3 / I_1$  and for output 3 is  $-I_4 / I_1$ .

. The reason for The minus sign in the gain of the third output is that these are mirrored by CM9 and CM10 before they are added.

The complete circuit for a three output programmable current conveyor is provided in Figure.2.6. It is a detailed circuit for the simplified schematic of Figure 2.5. In this circuit, the gain control currents, are  $I_c$ ,  $I_{c1}$ ,  $I_{c2}$  and  $I_{c3}$ . These are built from current mirrors similar to CM1- CM8 in the last Figure. Only the third output is provided a negative gain.



**Fig 2.5. a) Input buffer (  $I_1 = I_2 < I_{IN}$  ). B) Symbol for four outputs programmable current mirror.**



(C)

Fig 2.5.C) Simplified schematic for the MOPCC.





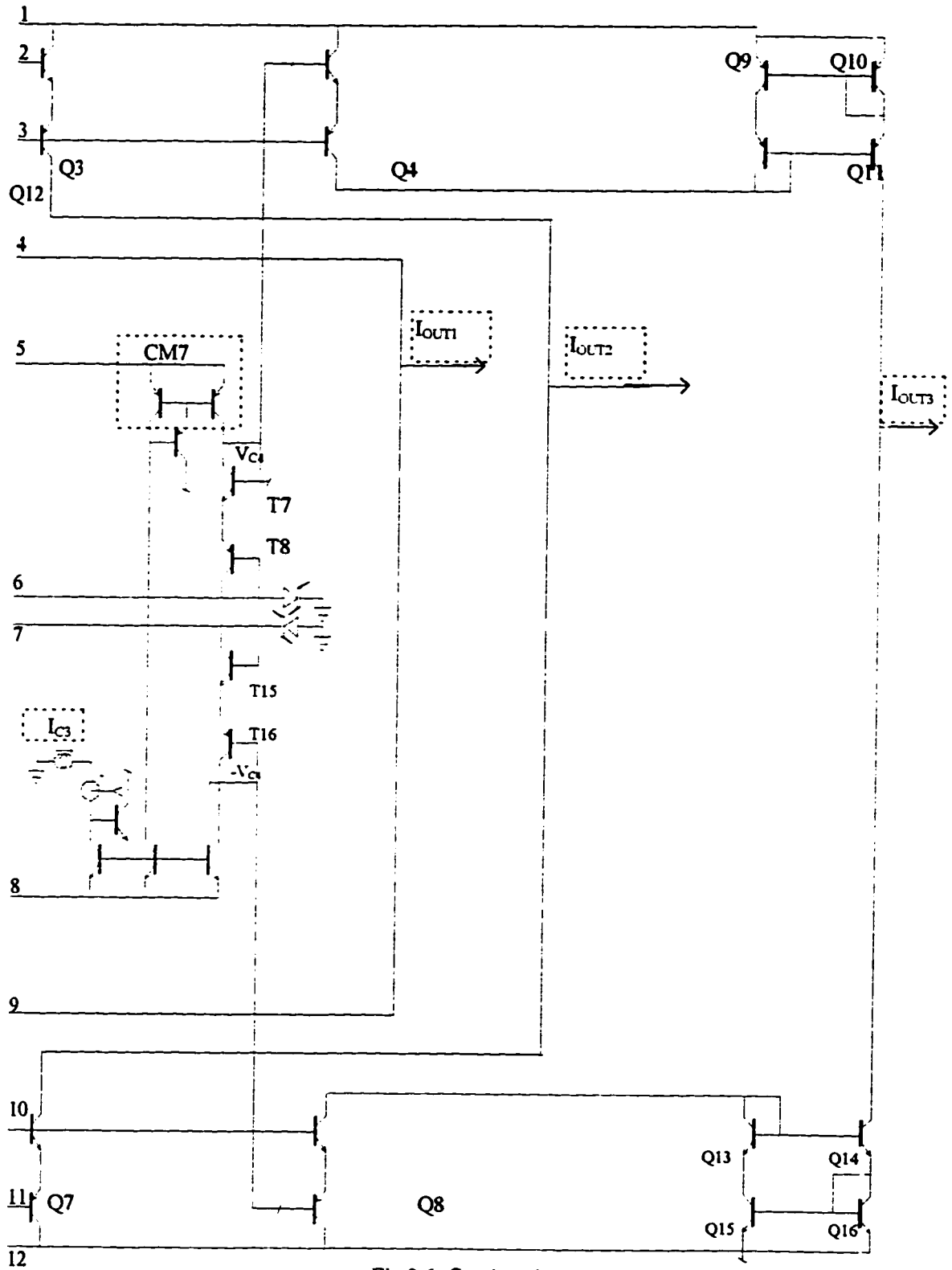


Fig.2.6. Continuation

Transistors  $T_1$ -  $T_8$  and  $T_9$  - $T_{16}$  form the upper and lower parts of the diodes network respectively. Current mirrors used to obtain a negative gain for the fourth output are formed using transistors  $Q_9$  - $Q_{12}$  and  $Q_{13}$  - $Q_{16}$  for positive and negative mirrors respectively. Finally, to obtain a MOPCC, a 741 Op Amp must be connected as an input buffer as shown in Figure 2.5 (b). As a consequence, two zener diodes were used to provide enough biasing for the Op Amp.

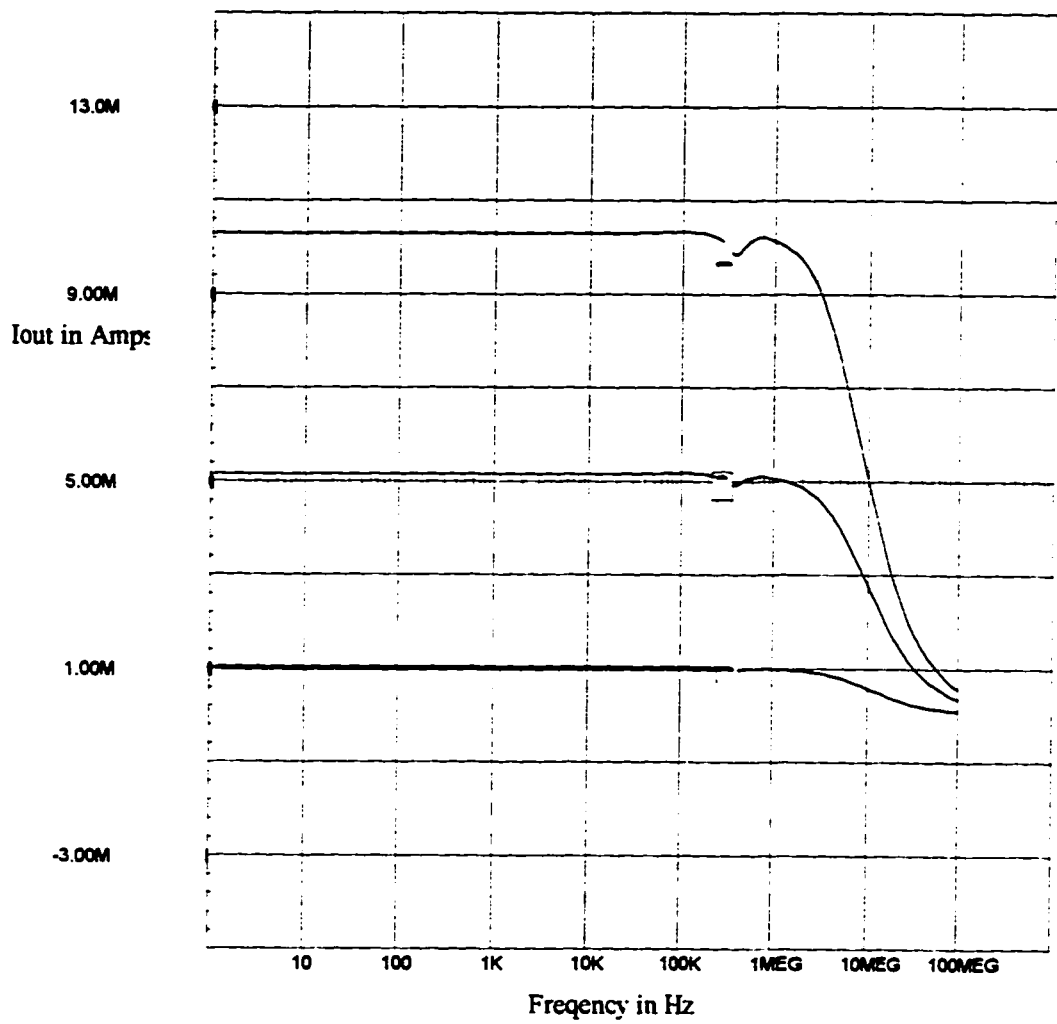
The circuit frequency response, together with the input output characteristics, obtained using ICAPS circuits simulation program, is shown in Figures 2.7, 2.8 and 2.9. Transistors used for simulation are the NPN 2N2222, and the PNP 2N2905. A maximum error of 5%, with respect to the ratio of the corresponding control currents, is observed in the gain. To Eliminate bandwidth limitations of the 741 Op Amp, it was replaced by the other class AB buffer of Figure.2.5- (a). Results show a bandwidth increase from 1 MHz to 10 MHz.

**2.3.2 Comparison with other results.** In this section the modified PGCM will be compared with the original one found in [1]. To start with, it is clear that the frequency response, obtained by simulation, of the original circuit is higher than the one obtained here. However, notice that in the original circuit the number of current sources that are considered to be ideal is large. On the other hand, all current sources in our circuit are represented by current mirrors. This will certainly have its reflection on the frequency

response of our circuit. All internal capacitances of transistors used to build these current mirrors will have their own effect on the final shape of the frequency response.

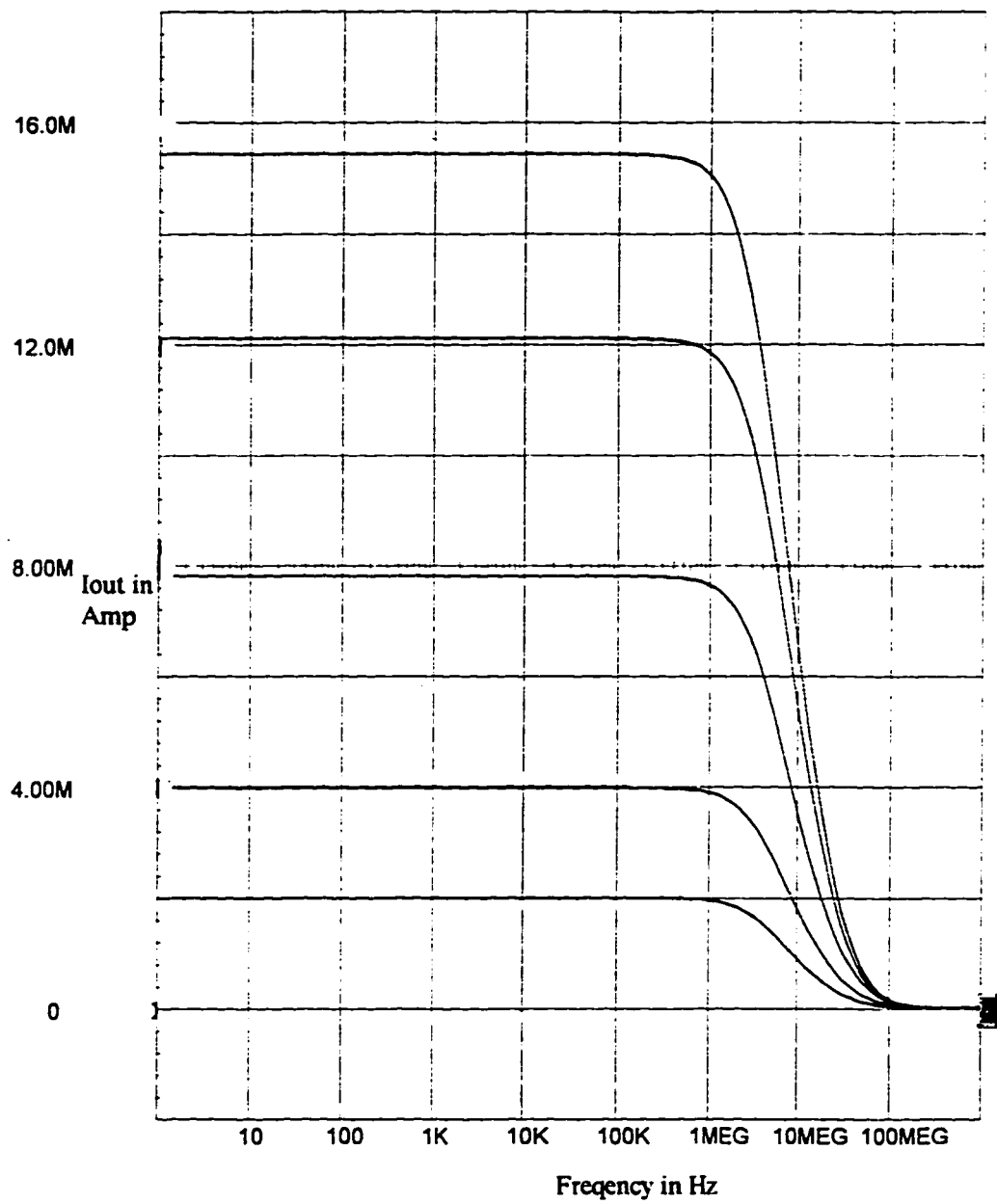
In the circuit presented in [1], both  $I_1$  and  $I_2$  are mirrored five times in the whole circuit. This will affect the final accuracy of the circuit gain. This point was totally ignored by the authors of [1]. No simulation or experimental work was presented to show the accuracy of the circuit gain. In our circuit, however, these two currents are mirrored two times at most. Also, a gain of 16 was obtained with an error of 3.7 %. higher gains are possible but ignored because of the relatively higher error. In the case of the circuit in [1], no gain higher than 10 was shown.

Another feature of our circuit is its ability to provide multiple outputs. The number of these is limited by the accuracy of the single output PGCM. The larger the number of outputs is, the lower the gain accuracy becomes. For the circuit in [1], it is impossible to obtain any additional outputs because of the way by which the currents in the control circuit are arranged. Finally, it was found experimentally that the beta value of the PNP transistor used for simulation in [1] is very low and not acceptable at all for implementing the linear single output PGCM.



*Gain = 1,5 and 10 upward.*

**Fig 2.7.** Gain - frequency characteristics of the PCC with a 741 Op Amp connected as a unity gain amplifier.



*Gain = 2, 4, 8, 12 and 16 upward, ( $I_1=I_2=0.5\text{mA}$ .)*

**Fig 2.8. Gain-frequency characteristics of a PCC with the buffer of a CFOA instead of the OP AMP**

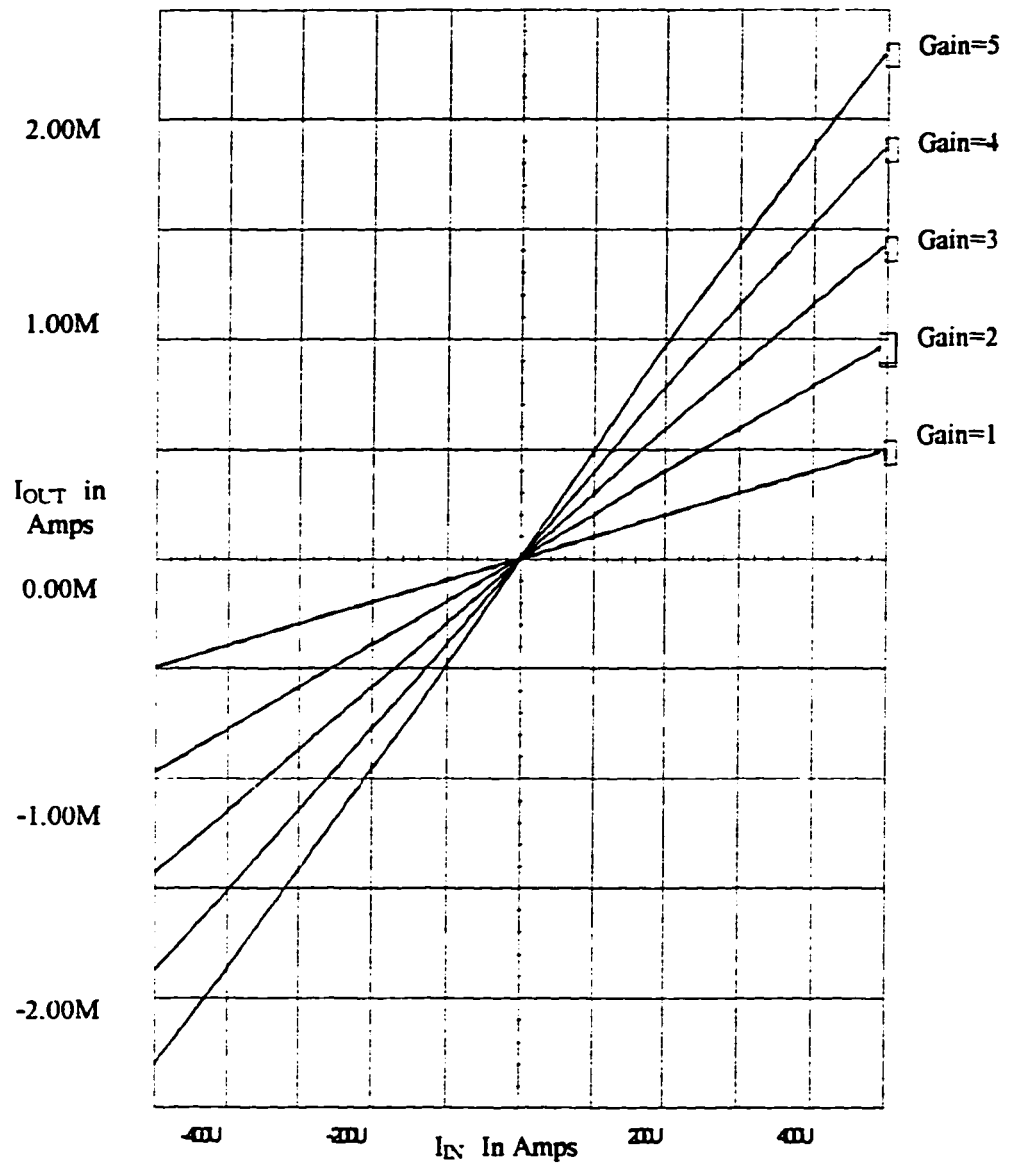


Fig 2.9. Input output characteristics ( with an Op Amp).

## 2.4 ANALOG SIGNAL PROCESSING USING PCC'S

**2.4.1- Universal Filter Design** Using one PCC together with five passive elements only a lowpass / bandpass filter can be obtained from one circuit. Such a circuit is shown in Figure 2.10.

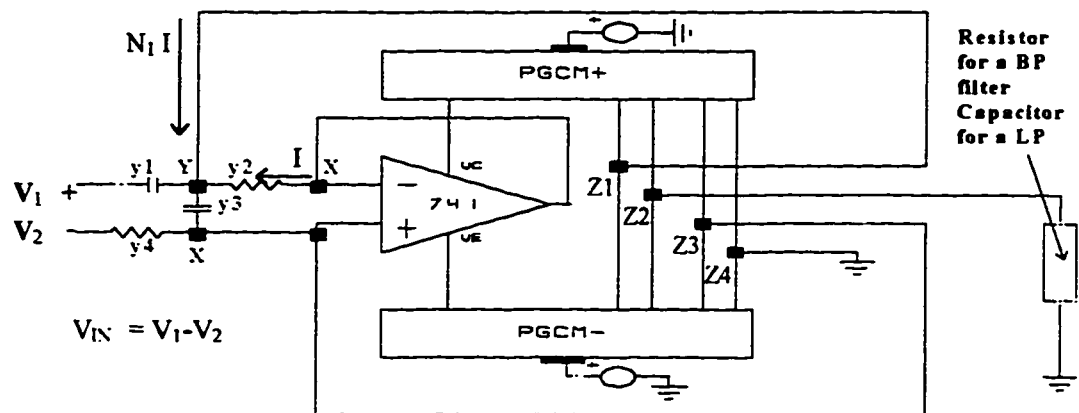


Fig 2.10. Programmable LP & BP filter

Let  $N_1$  ,  $N_2$  ,  $N_3$  ,  $N_4$  represent gains of the four different outputs respectively.

Assuming Ideal OP AMP, then, applying KCL and KVL, we get

$$I = (X - Y) * Y_2 \quad (2.3)$$

$$(Y - V_1) * Y_1 + (Y - X) * Y_3 = (N_1 + 1)I$$



$$\begin{aligned}
&\Rightarrow (Y - V_1) * Y_1 - (I / Y_2) * Y_3 = (N_1 + 1)I \\
&\Rightarrow I [Y_3 + (N_1 + 1) Y_2] = (Y - V_1) * Y_1 Y_2
\end{aligned} \tag{2.4}$$

Also,

$$\begin{aligned}
N_3 I &= (X - V_2) Y_4 + (X - Y) Y_3 \\
&\Rightarrow N_3 I = (X - V_2) Y_4 + (I / Y_2) * Y_3 \\
&\Rightarrow I (N_3 * Y_2 - Y_3) = (X - V_2) Y_4 Y_2
\end{aligned} \tag{2.5}$$

From 2.4 and 2.5 into 2.3, we get :

$$\begin{aligned}
I / Y_2 &= I (N_3 * Y_2 - Y_3) / Y_4 Y_2 + V_2 - I [Y_3 + (N_1 + 1) Y_2] / Y_1 Y_2 - V_1 \\
&\Rightarrow I [Y_1 Y_4 - (N_3 * Y_2 - Y_3) Y_1 + Y_4 [Y_3 + (N_1 + 1) Y_2]] = -V_{12} * Y_1 Y_2 Y_4 \\
&\Rightarrow \frac{I}{V_{12}} = \frac{-Y_1 Y_2 Y_4}{[Y_1 Y_4 - (N_3 * Y_2 - Y_3) Y_1 + Y_4 [Y_3 + (N_1 + 1) Y_2]]}
\end{aligned} \tag{2.6}$$

Let  $Y_1$  and  $Y_3$  be capacitive while  $Y_2$  and  $Y_4$  represent resistors. Then

$$\frac{I}{V_i} = \frac{-SC_1 G_2 G_4}{S^2 C_1 C_3 + SC_1 G_4 + SC_3 G_4 - SC_1 G_2 N_3 + (N_1 + 1) G_4 G_2}$$

Let Den = Denominator of  $I / V_i$ . Then:

$$V_{BP} / V_i = (N_2 R_{out}) / \text{Den} \tag{2.7}$$

$$V_{LP} / V_i = (N_1 C_1 G_2 G_4 / C_{out}) / \text{Den} \tag{2.8}$$

For both outputs ;

$$\omega_0^2 = \frac{N_1 + 1}{R_2 R_4 C_1 C_3} \quad (2.9)$$

$$BW = \left( \frac{1}{R_4 C_1} + \frac{1}{R_4 C_3} \right) - \left( \frac{N_3}{R_2 C_3} \right) \quad (2.10)$$

$$\text{Gain of BPF is } G_{BP} = \frac{N_2 R_{OUT} R_4 R_2}{R_2 (C_1 + C_3) - R_4 C_1 N_3} \quad (2.11)$$

$$\text{Gain of LPF is } G_{LP} = \frac{C_1}{(N_1 + 1) C_{out}} \quad (2.12)$$

$N_1$  controls the center frequency and  $N_3$  controls the filter bandwidth independently. However, the gain is independently controllable only for the LP output. Notice that the circuit accepts both differential and single ended inputs and is temperature independent which makes it more versatile. Finally, a word of caution must be mentioned regarding the minus sign at the denominator of both filters equations. This sign may result in instability or large sensitivity to filter parameters. For this reason, another terminal ,  $Z_4$  , whose current gain is negative, is provided. Instead of feeding back the output of  $Z_3$  to the impedance  $y_4$ , this terminal can be used. This results in replacing every  $N_3$  in all previous equations by  $N_4$  which is negative and thus ensures the stability of the resulting filter.

Simulations results, using ICAPS, of both LP and BP filters are presented in Figures 2.11 and 2.12 respectively. As can be seen, changing  $N_3$  alone results in changing the bandwidth of the filter as expected from expressions of the BW for both filters. Notice the change of the gain of the BP filter when  $N_3$  is varied. This change, though not desired, is well expected from the gain expression of the BP filter. A disadvantage of this circuit is the need for high currents in order to increase the center frequency linearly. In all simulations, a maximum error of 8% was obtained between theoretical and simulated values of the bandwidths which is mainly due to the error of the programmable current mirror. These errors can be reduced if high beta transistors or more accurate mirror structures were used.

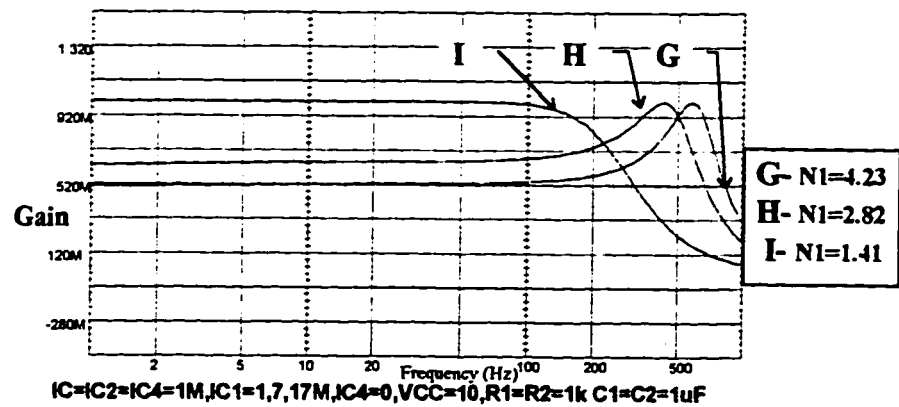
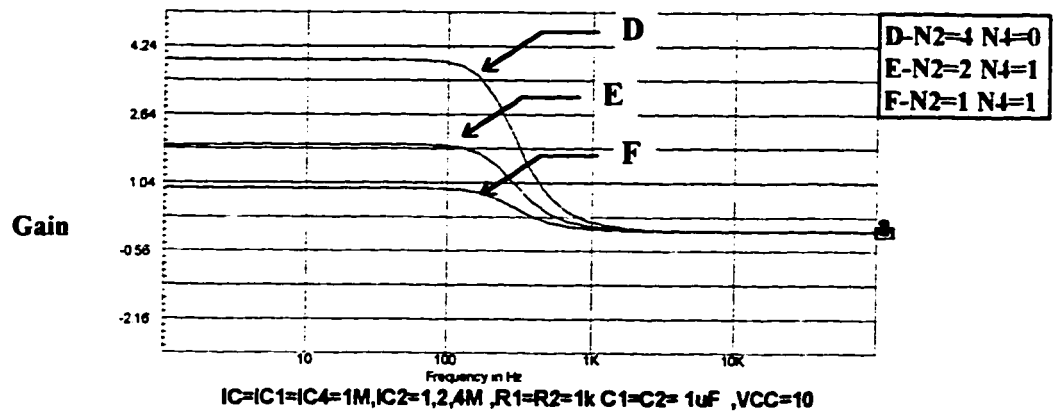
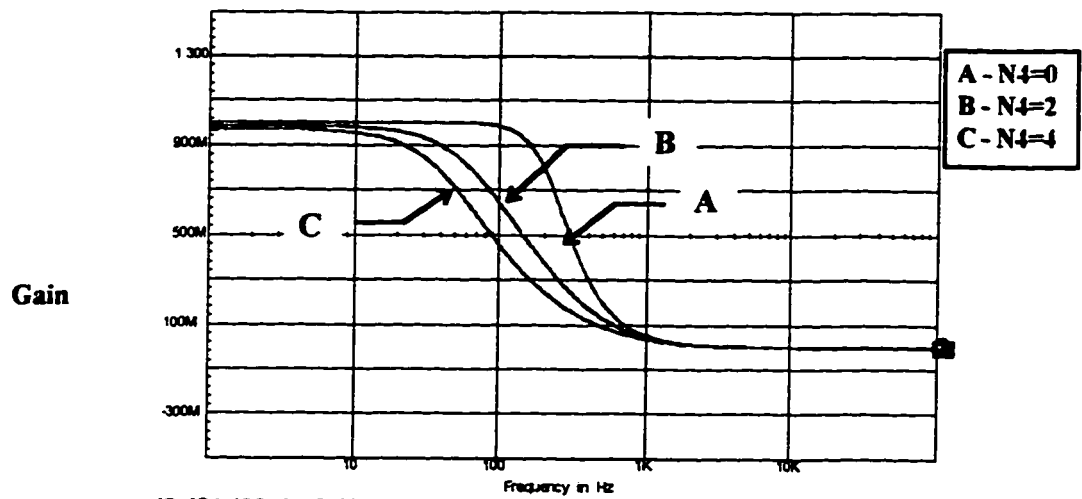
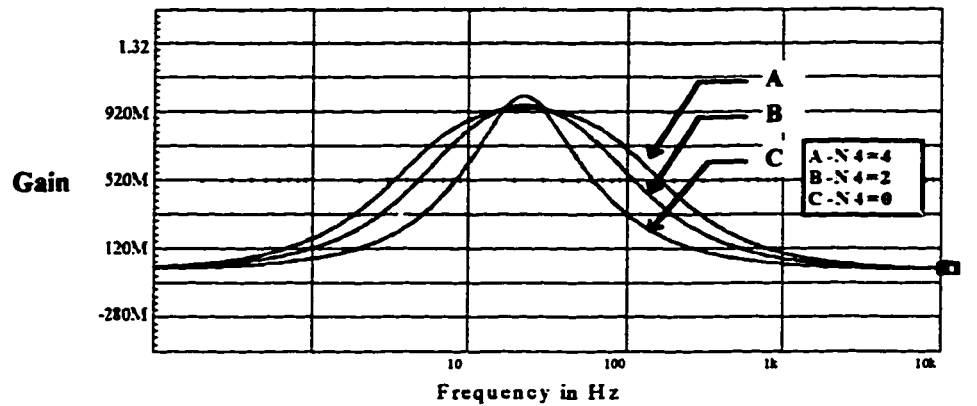
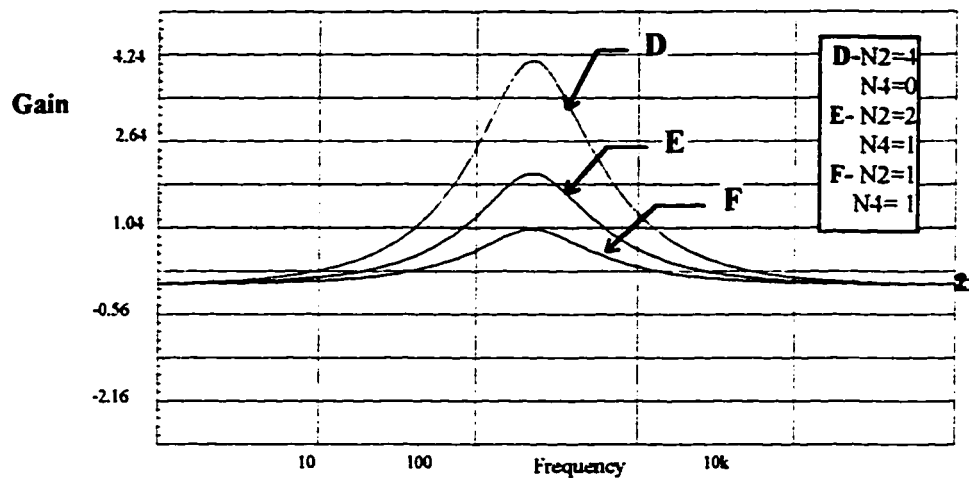


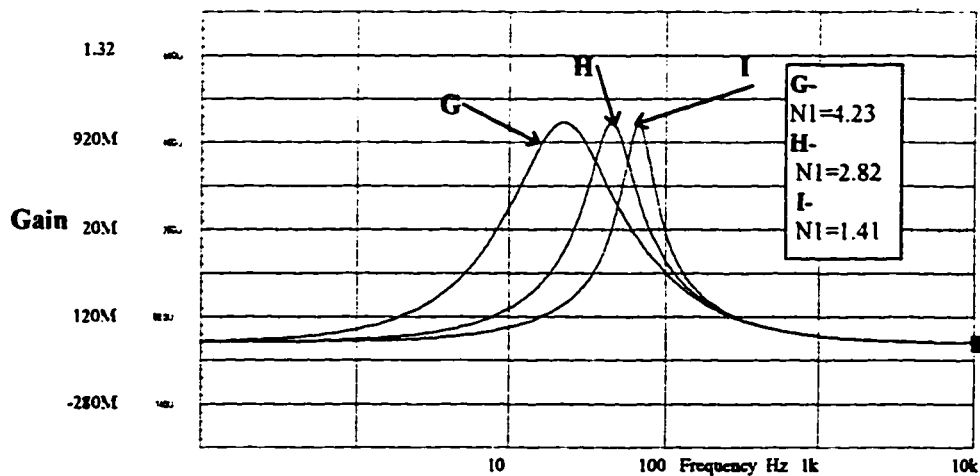
Fig 2.11. Programming of Q, Gain, Center frequency of the LP filter.



IC=IC1=IC2=IC3=1mA, IC4=0,2,4 mA, R1=R2=1k C1=C2= 1uF, VCC=10, VIN=0.5Vp

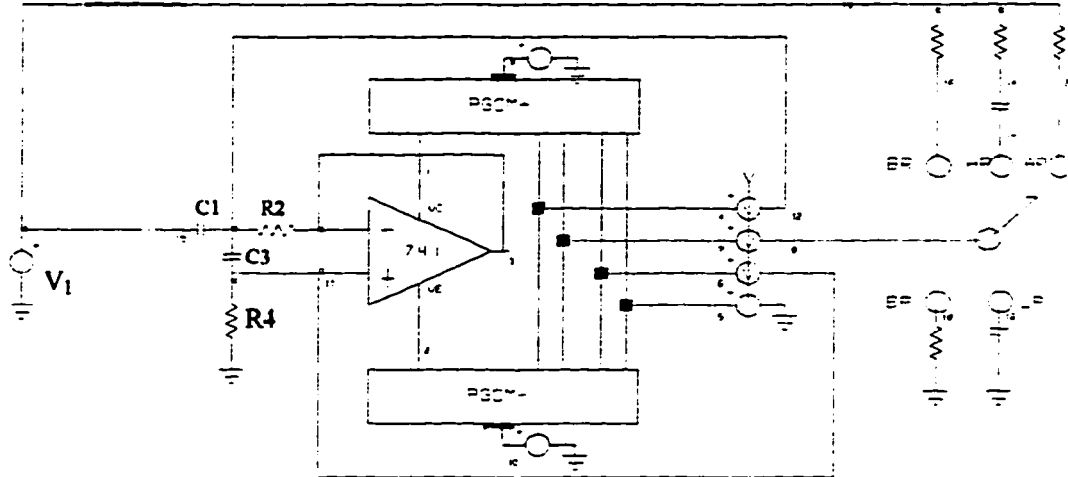


IC=IC1=IC3=IC4=1mA IC2=1,2,4mA R1=R2=1K C1=C2=1uF



IC=IC2=IC3=IC4=1mA IC1=1,7,17mA R1=R2=1k C1=C2=1uF

Fig 2.12. Programming of Q, Gain, Center frequency of the BP filter.



**Fig 2.13. Programmable universal filter\ oscillator**

Addition of a passive feedback from a Z terminal to the input source,  $V_1$ , can be used to obtain more transfer functions, see figure 2.13. With this topology, the following functions are obtained:

Case 1: One capacitor and resistor are feedback

$$T = \frac{s^2 C_1 C_3 + s C_1 G_4 + s C_3 G_4 - s C_1 G_2 N_3 - s C_1 G_2 G_4 R_F N_2 - C_1 G_2 G_4 N_2 / C_F + (N_1 + 1) G_4 G_2}{s^2 C_1 C_3 + s C_1 G_4 + s C_3 G_4 - s C_1 G_2 N_3 + (N_1 + 1) G_4 G_2}$$

Under the following two conditions:

$$1- C_1 G_4 + C_3 G_4 = C_1 G_2 N_3 + C_1 G_2 G_4 R_F N_2$$

$$2- C_1 N_2 / C_F = (N_1 + 1)$$

We obtain a HP function in the form of :

$$T_{HP} = \frac{S^2 C_1 C_3}{S^2 C_1 C_3 + S C_1 G_4 + S C_3 G_4 - S C_1 G_2 N_3 + (N_1 + 1) G_4 G_2} \quad (2.13)$$

A band reject filter can also be obtained from the same point with the first condition only:

$$C_1 G_4 + C_3 G_4 = C_1 G_2 N_3 + C_1 G_2 G_4 R_F N_2 .$$

Which results in the following transfer function

$$T_{BR} = \frac{S^2 C_1 C_3 - C_1 G_2 G_4 N_2 / C_F + (N_1 + 1) G_4 G_2}{S^2 C_1 C_3 + S C_1 G_4 + S C_3 G_4 - S C_1 G_2 N_3 + (N_1 + 1) G_4 G_2} \quad (2.14)$$

Case 2: Resistive feedback only

$$T = \frac{S^2 C_1 C_3 + S C_1 G_4 + S C_3 G_4 - S C_1 G_2 N_3 - S C_1 G_2 G_4 R_F N_2 + (N_1 + 1) G_4 G_2}{S^2 C_1 C_3 + S C_1 G_4 + S C_3 G_4 - S C_1 G_2 N_3 + (N_1 + 1) G_4 G_2}$$

$$\text{Which becomes; } T_{BR} = \frac{S^2 C_1 C_3 + (N_1 + 1) G_4 G_2}{S^2 C_1 C_3 + S C_1 G_4 + S C_3 G_4 - S C_1 G_2 N_3 + (N_1 + 1) G_4 G_2} \quad (2.15)$$

If the same previous condition is met.

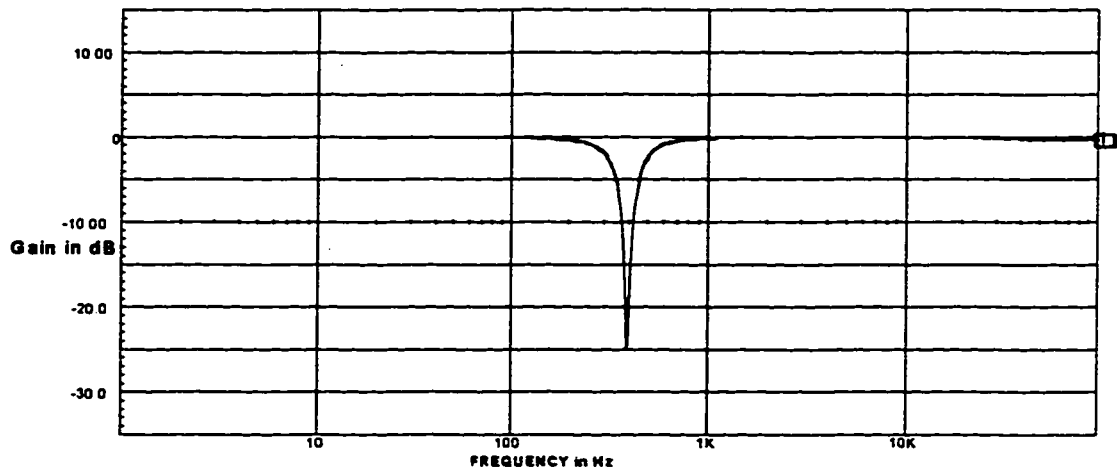
Also, if:  $C_1 G_4 + C_3 G_4 - C_1 G_2 N_3 = 0.5 * C_1 G_2 G_4 R_F N_2$ .

Then, the following AP function is obtained:

$$T_{AP} = \frac{S^2 C_1 C_3 - S C_1 G_4 - S C_3 G_4 + S C_1 G_2 N_3 + (N_1 + 1) G_4 G_2}{S^2 C_1 C_3 + S C_1 G_4 + S C_3 G_4 - S C_1 G_2 N_3 + (N_1 + 1) G_4 G_2} \quad (2.16)$$

For all previous filters, if the feedback from Z3 to the resistance R4 is replaced by a feedback from Z4 to R4, then more stable filters are obtained. This is due to the negative gain of terminal Z4. This was taken into consideration when simulations of BR, HP and AP filtering functions were done. Results of these simulations are shown in figure. 2.14. For the BR function, the function reaches zero at a frequency of 160 Hz although this is not clear in the figure. Also, a small nop appears in the amplitude response of the AP filter at the same frequency. This is due to the inaccuracy of the PCM which results in unsatisfying the conditions exactly. Theoretical derivations show a cutoff frequency of 159 Hz which is in excellent agreement with the value obtained by simulation.





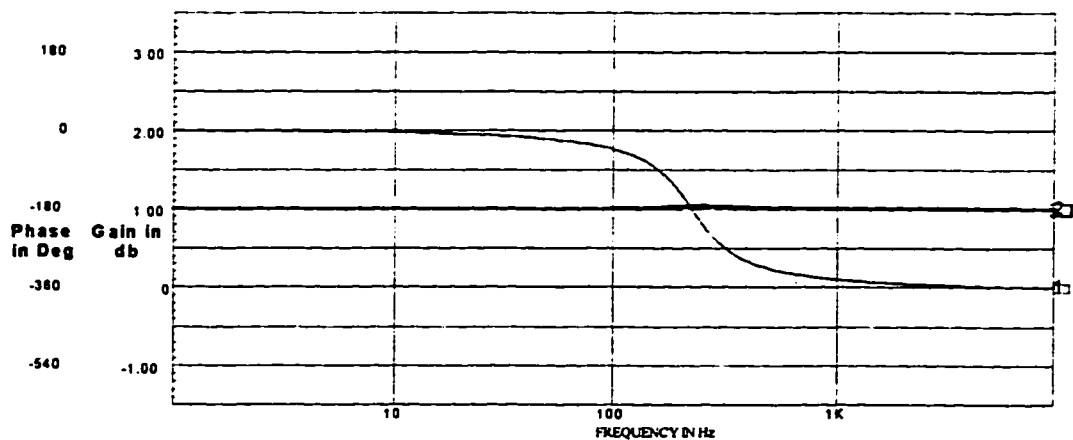
### 1) Band-Reject Filtering

$IC=IC_2=IC_4=1mA$   $IC_1=5mA$   $R_2=R_4=RF=1k$   $C_1=C_3=1\mu F$  ( Resistive feedback )



### 2) Highpass Filtering

$IC=IC_2=IC_4=1mA$   $IC_1=0mA$   $R_2=R_4=RF=1k$   $C_1=C_3=CHP=1\mu F$



### 3) Allpass Filtering

$IC=IC_2=IC_4=IC_1=1mA$   $R_4=R_2=1k$   $RF=2k$   $C_1=C_3=1\mu F$

Fig 2.14. Bandreject, highpass and allpass outputs using one MOPCC with different feedback elements to the input.

**2.4.2- Oscillator Design** The circuit in figure 2.13, without any component changes, is capable of generating oscillations. This is achievable when the coefficient of  $s$  in the denominator is made equal to zero. The frequency of oscillation can be changed automatically through  $N1$  if the condition of oscillation is always met by  $N3$ . If this condition is satisfied, a current controlled oscillator is obtained. However, one should take care of the current transfer ratio resulting from extending the current mirror to give three outputs. The amplitude of the resulting sinusoidal signal can also be varied easily with  $N2$ .

This oscillator provides two orthogonal signals at the same time. They are at the same previous bandpass and lowpass outputs. The amplitudes of these two signals are controllable via two different variables,  $N1$  and  $N2$ . Moreover, if multiphase output signals are desired, the output oscillating current at  $Z2$  can be mirrored into different RC phase shaping networks. Results showing the programmability of this oscillator, are shown below.

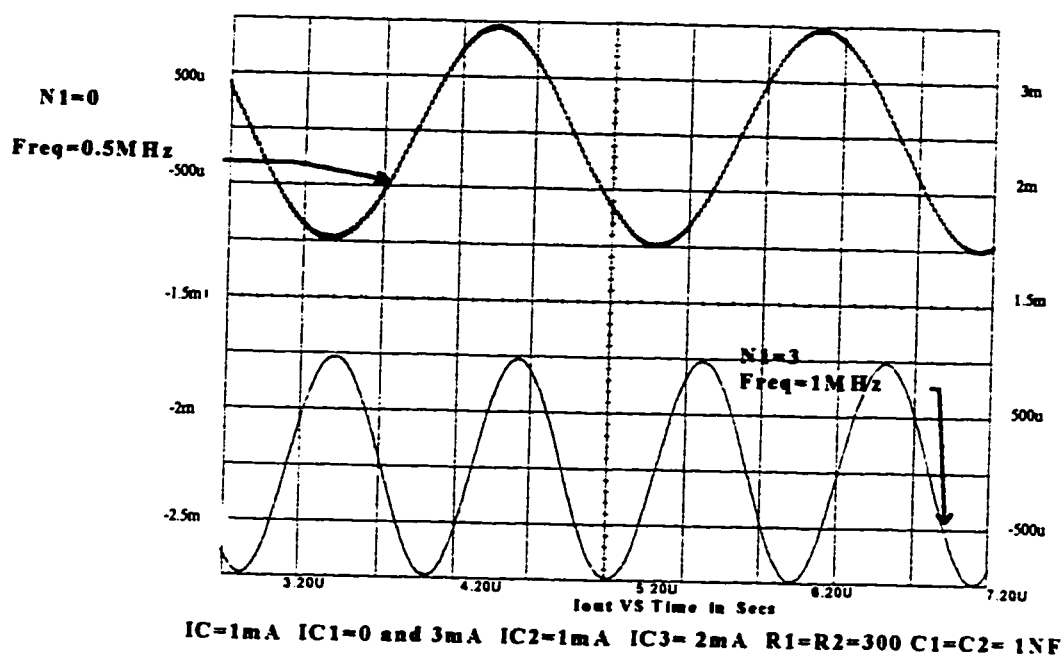


Fig 2.15. Changing N1 results only in doubling the frequency.

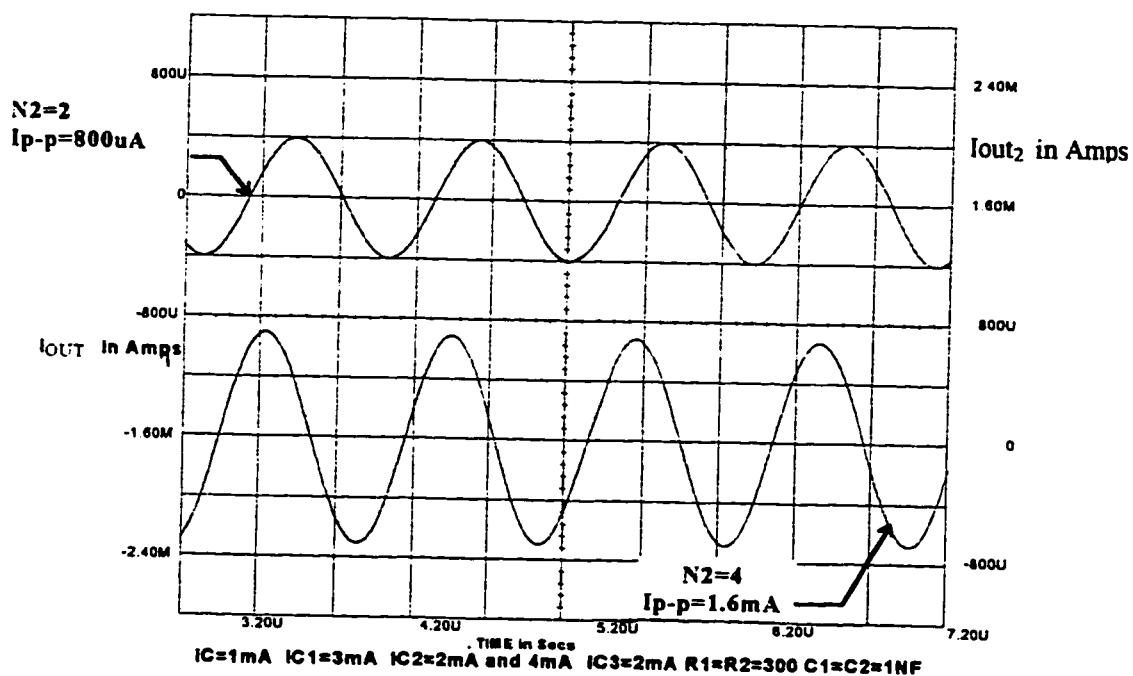


Fig 2.16. Changing N2, amplitude can be controlled linearly.

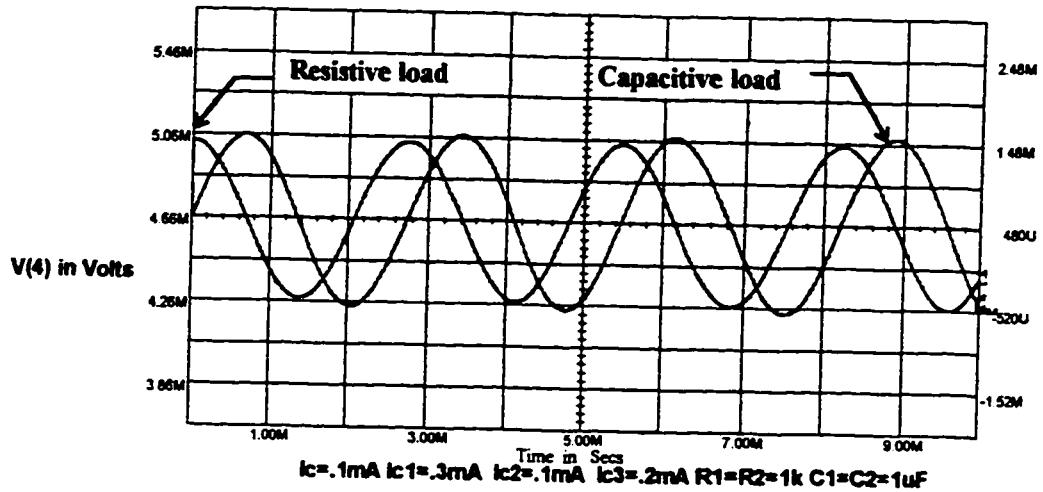


Fig 2.17. Programming of the phase of the oscillator using different R-C loads.

From previous analysis, it can be shown that:

$$W_0^2 = \frac{N_1 + 1}{R_2 R_4 C_1 C_3}$$

A frequency of 470 KHz was obtained when  $N_1$  was set to zero while it is expected, from the expression of  $W_0$ , to obtain a 0.5 Mhz frequency. This corresponds to an error of 6%.

Similarly, an error of 13% in the resulting frequency occurred when  $N_3$  was set to 3. As  $N$  values are increased, errors are expected to increase too. This is due to the errors of the programmable current mirror used to construct the MOPCC. In addition, the more

the frequency is increased, the more the effect of internal capacitances and resistances of the MOPCC becomes apparent. Another feature of the circuit is the programmability of its output amplitude via  $N_2$ . This programmability, as shown in figure.2.16 is linear. Finally, figure 2.17 shows how the phase of the resulting signal can be controlled by changing the load composed of an RC network . Also, the availability of a grounded resistor makes it possible to control the gain of the resulting frequency over a wider range by changing the value of this resistance. Such a resistance can be replaced by an OTA connected as a resistance. Changing the control current of the OTA results in changing the value of its resistance automatically.

## CHAPTER 3

# MULTIPLICATION, DIVISION, AND PIECEWISE LINEAR APPROXIMATION

### 3.1 INTRODUCTION

The status of the current VLSI technology is advancing very rapidly and extremely more compact circuits, both analog and digital, can be fabricated on the same chip. It is becoming more evident that analog VLSI signal processing systems constitute a potential future trend. Analog nonlinear circuits have their wide range of applications in analog signal processing systems. These include telecommunication and electronic systems, instrumentation, wave generation, modulation, computational circuits, etc.

After considering the use of programmable current mirrors in linear signal processing, some nonlinear applications are proposed in this chapter. To start with, linear

programmable current mirror (PCM) based multipliers, dividers and piecewise linear function approximating circuits are discussed.

### 3.2 NONLINEAR APPLICATIONS USING LINEAR PCM'S

#### 3.2.1 Multipliers Bipolar PCM's can be used as two quadrant multipliers.

Figure.3.1 shows the circuit diagram of a two quadrant multiplier. Control voltages  $V_{c1}$  and its negative are generated across diode connected transistors  $Q_2$  - $Q_4$  and  $Q_6$  - $Q_8$  respectively by  $I_{IN2}$  which is fed from CM1 and CM2 current mirrors.  $V_{c2}$  and its negative are produced by  $I_{IN}$  the same way using CM3 and CM4 mirrors. Form Figure 3.1, it can be seen that control voltages can be expressed as

$$\left. \begin{array}{l} V_{c1} = 2V_T \ln [ I_{IN2} / I_s ] \\ V_{c2} = 2V_T \ln [ I / I_s ] \end{array} \right\} \dots\dots\dots (3.1)$$

Applying KVL around the loop of transistors  $Q_9$  - $Q_{13}$ , we get

$$\begin{aligned} 2V_T \ln [ I_{OUT} / I_s ] - 2V_T \ln [ I_{IN1} / I_s ] &= V_{c1} - V_{c2} \\ \Rightarrow I_{OUT} / I_{IN1} &= \text{Exp} [( V_{c1} - V_{c2} ) / (2 V_T)] \dots\dots\dots (3.2) \end{aligned}$$

Substituting from 3.1, we get

$$I_{OUT} / I_{IN1} = I_{IN2} / I$$

$$\text{Thus } I_{OUT} = (I_{IN1} * I_{IN2}) / I \dots\dots\dots (3.3)$$

Thus, one quadrant multiplication is obtained when the current  $I$  is kept constant.

By connecting the negative of  $V_{c1}$  and  $V_{c2}$  to the lower current mirror, composed of transistors  $Q_{14}$ - $Q_{18}$ , and connecting the input signal to both upper and lower mirrors, we obtain a two quadrant multiplier. This is because the input current is processed when it is positive, through upper main mirror, and when it is negative, through lower main current mirror.



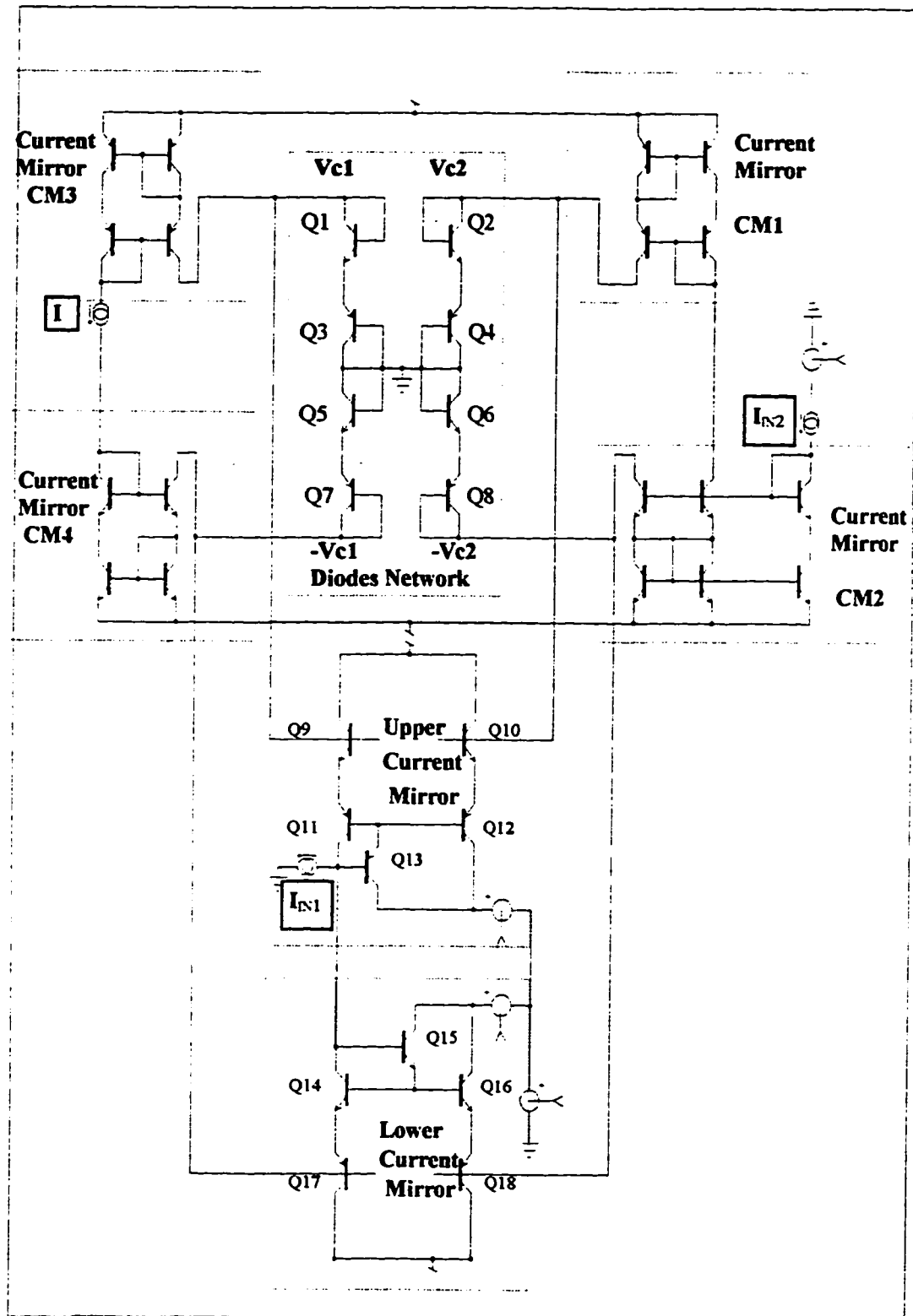


Fig 3.1. Two quadrant multiplication circuit.  $I_{N1} = 10 \sin(\omega t)$  mA with  $f = 10$  MHz..  
 $I_{N2} = 1 + \sin(\omega t)$  mA with  $f = 1$  MHz.  $I_2 = 1$  mA.

Using ICAPS, simulation results of multiplying a sinusoidal signal having a frequency of 10MHz with another one of frequency 1MHz are shown in Figure 3.2. The low frequency input is DC shifted by the peak value in order to obtain a positive wave. The Amplitude spectrum of the output shows a very low harmonic distortion which could be due to mathematical errors of the simulation program itself. Since this circuit is actually a PGCM, with control currents being replaced by the two input currents, then its main features are the same as mentioned in section 2.2.

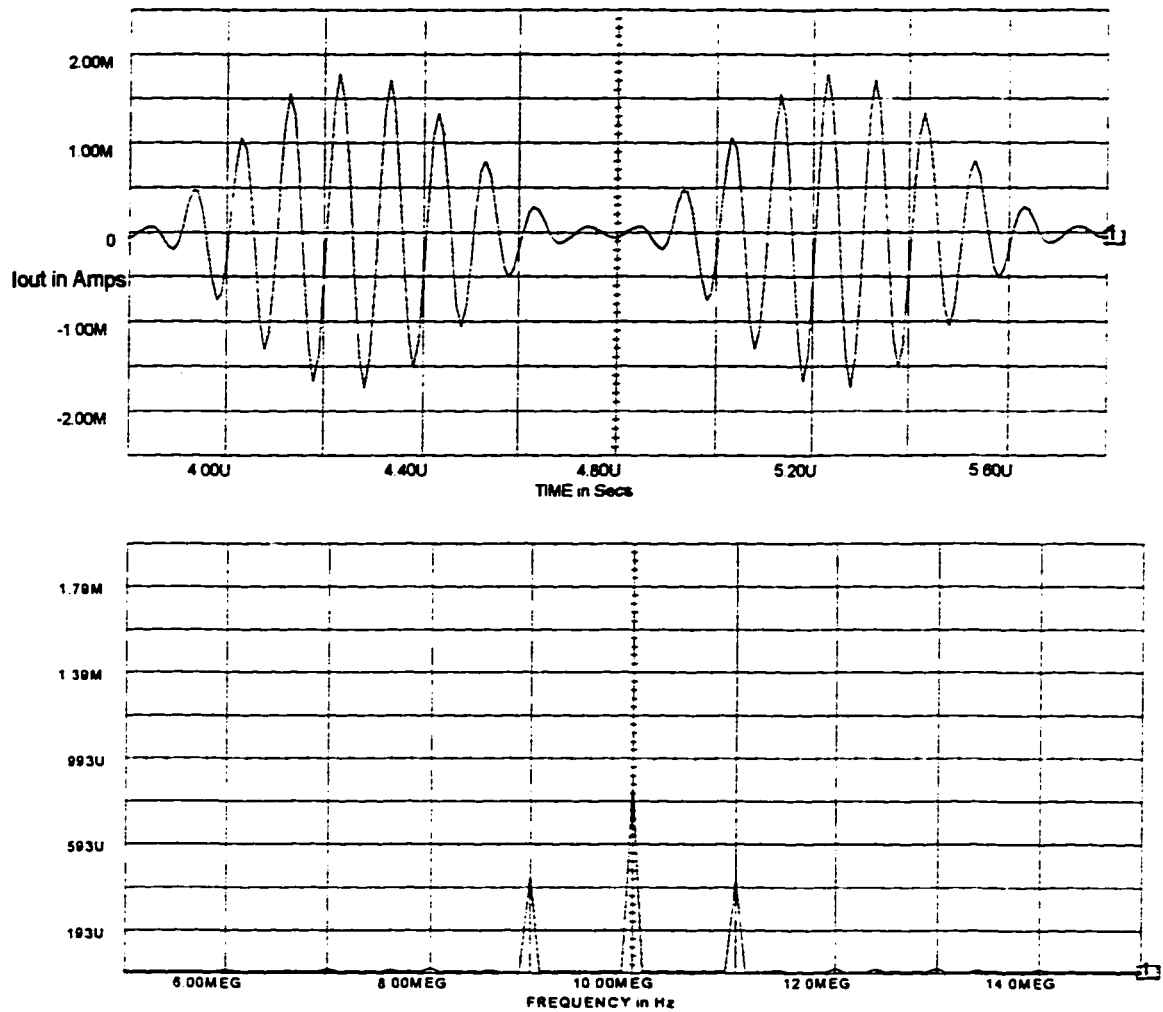


Fig (3.1). Result of multiplying two sinusoidal signals with  $f_1 = 10\text{MHz}$  and  $f_2 = 1\text{mhz}$ . A) in time domain  
B) in frequency domain.

**3.2.2 One-Over Circuit** Using the upper mirror of the previous circuit only a one over circuit can be obtained if currents  $I$  and  $I_{IN2}$  are interchanged. This can be explained from the equation (3 ) used previously to obtain a one-quadrant multiplier. From this equation, the gain of the resulting circuit becomes :

$$\text{Gain} = \frac{I}{I_{N2}}$$

$$I_{OUT} = \text{Gain} * I_{N1} = \frac{I}{I_{N2}} * I_{N1} \quad (3.4)$$

Where  $I$  is a DC source and  $I_{N2}$  is the input signal.  $I_{N1}$  is the input to the main current mirror as shown in Figure.3.3.

Such a circuit was simulated using ICAPS with positive linear inputs having slopes of 0.25, 0.5, and 1. The output signals together with their reciprocal are shown in Figure.3.4. Looking at the reciprocals of these outputs, it can be seen that these curves start linearly and then bend more and more as they approach their maximum. However, this bending does not exceed 8% of the input, the reciprocal of the theoretical output. This error occurs because output transistors start entering their cutoff region as the output becomes smaller and smaller. Also, all outputs are not expected to reach infinity, as expected mathematically, because of the nonlinearities of transistors as they enter the saturation mode. This leads us to the conclusion that the circuit is best suitable for an input range of 10u to 500uA. In comparison with other circuits in [32-36], it can be seen that the circuit exhibits a relatively wide input range. However, this is based on the availability of high beta transistors. The accuracy of this circuit is better than the one described in [33]. In addition, it occupies much smaller area. On the other hand, the circuit mentioned in [32] is capable of providing more than one input in addition to other operations that can be done

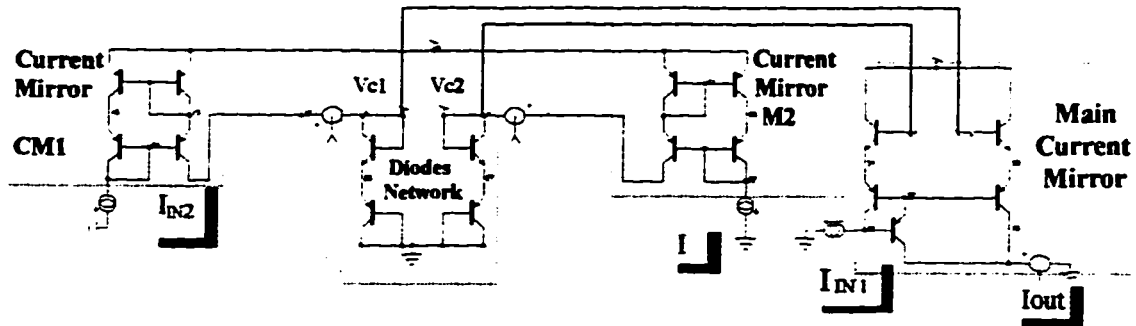
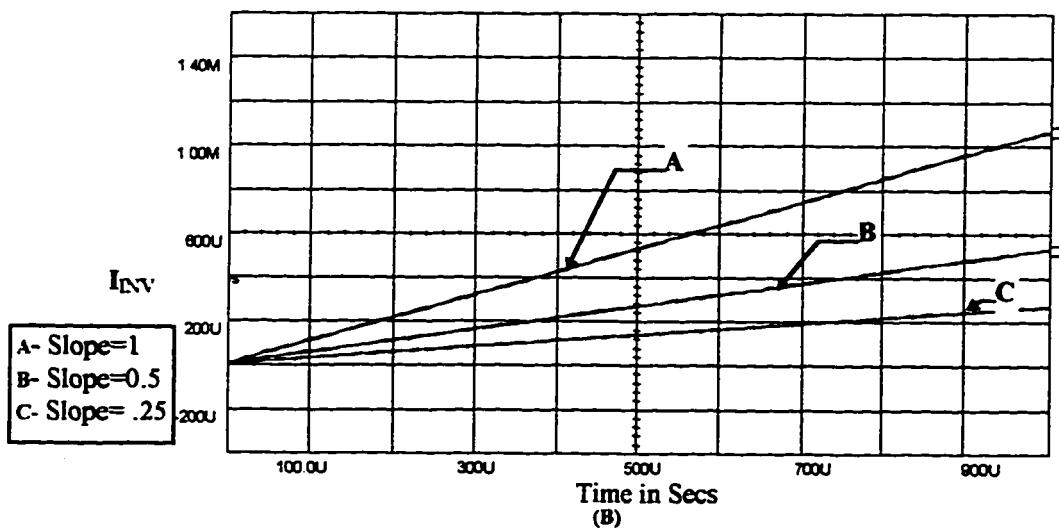
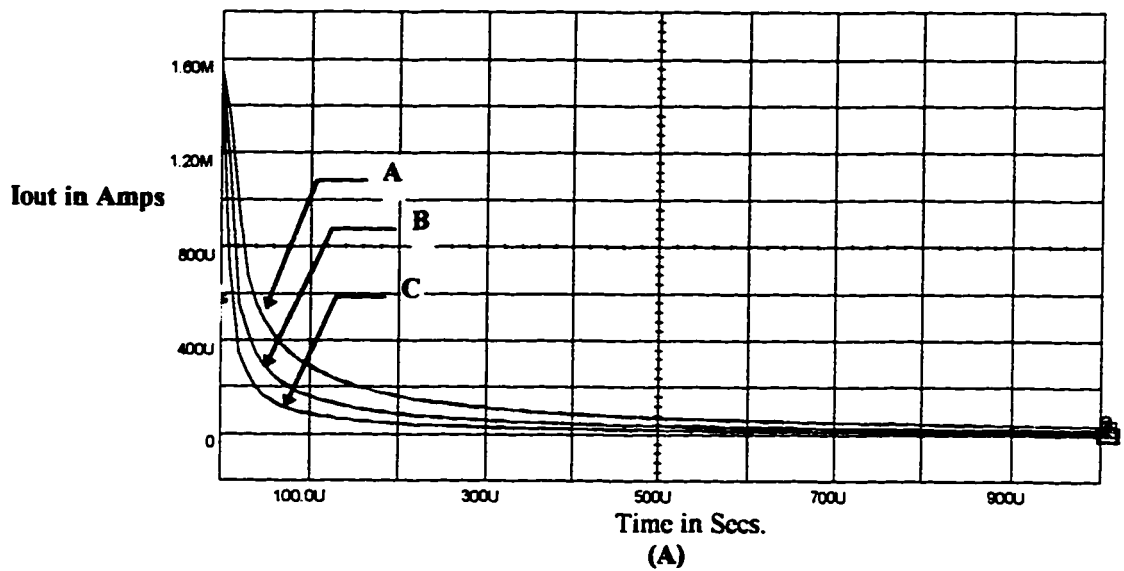


Figure 3.3. One over circuit.

Fig 3.4. (A) Outputs for linear inputs with slopes of A) 0.25 B) 0.5 C) 1.0 and  $I=1\text{mA}$   $I_{IN1}=10\mu\text{A}$ 

$$I_{OUT} = I / I_{IN2} * I_{IN1} \text{ where } I_{IN2} \text{ is the linear input}$$

(B) Scaled reciprocals of  $I_{OUT}$  Vs Time in Secs. ( $I_{INV} = I / I_{OUT} * I_{IN1}$ )

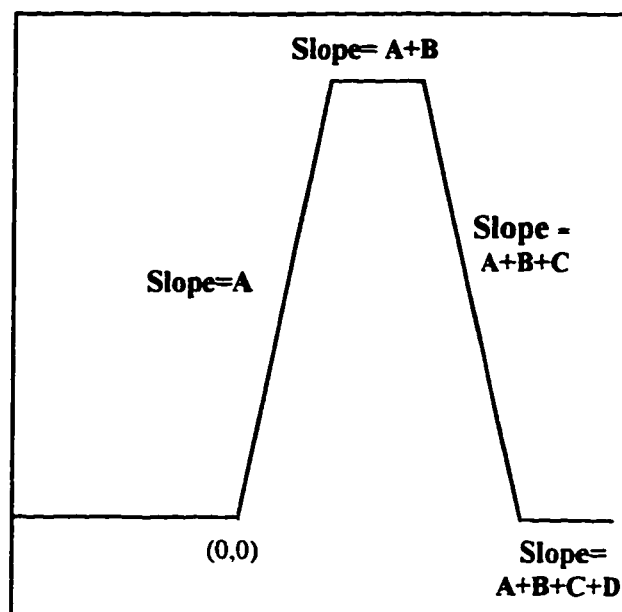
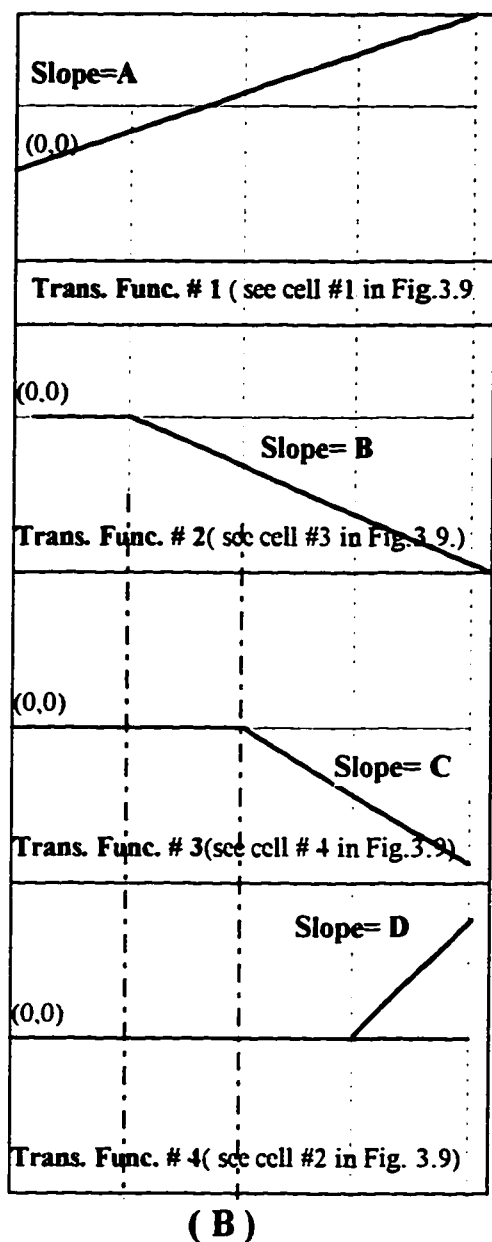
simultaneously with division. All available division circuits, including the proposed one in Figure 3.3 are capable of performing only two quadrant division. Other one-over circuits, based on the use of MOS transistors in their saturation region, are characterized by their lower power consumption and smaller input range. These circuits [35] are also smaller in area than our circuit because of the use of smaller number of MOS transistors. However, circuits based on MOS transistors are generally slower than their bipolar counterpart.

**3.2.3 Piecewise Linear approximation** Another application of programmable current mirrors is using them as building blocks to implement nonlinear functions. Since each PCM provides a linear relationship between its input and output, with a programmable slope, the addition of a number of such outputs yields the required nonlinear function, see Figure.3.5. The programmability of the PCM implies that no need for hardware changes whenever the required function is changed. Also this function could be made time varying, if desired, by making the control currents also varying in the same way. The number of PCM to be used in implementing a certain function is determined only by the required accuracy and the smoothness of the function.. Notice that the input range of the required function must be at most equal to the input range of the PCMs used to implement this function.

Unipolar PCM's can produce transfer functions with unipolar slopes only. These were considered in section 3.1 as one quadrant multipliers. The same circuit, with an

addition of a DC offset current at the input is shown in Figure.3.6 together with its symbol and characteristics curve. The breakpoint in the characteristics is obtained using this DC offset because the circuit will forbid the input current from entering until it becomes greater than this offset. In this way the breakpoint is programmed through  $I_{\text{offset}}$ .

If the required transfer function contains both positive and negative segments slopes, then, the two kinds of unipolar mirrors should be used in a way to reduce hardware implementation to the minimum. As an example, if  $A = D = 1$  and  $B = C = -1$ , see Figure (3.5), then we obtain a trapezoidal function as shown in the Figure.3.5. An implementation of this circuit, with minimum number of unipolar PCMs, together with its output is provided in Figures.3.7.and 3.8. Simulations show a good accuracy of the resulting transfer function.



**Fig 3.5. Piecewise linear function approximation method.**  
 The nonlinear function of (a) can be decomposed into the piecewise linear functions of (b)



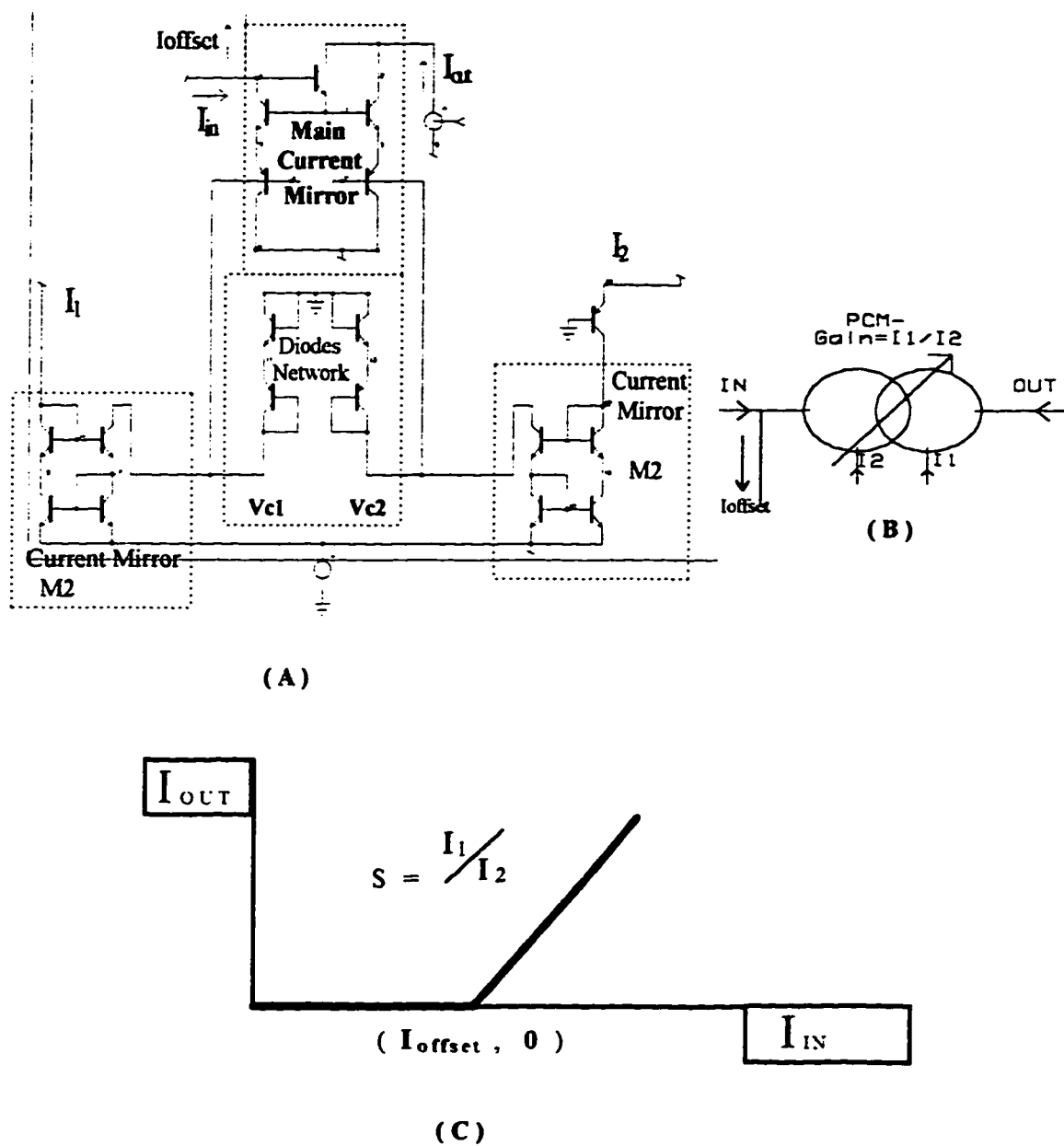
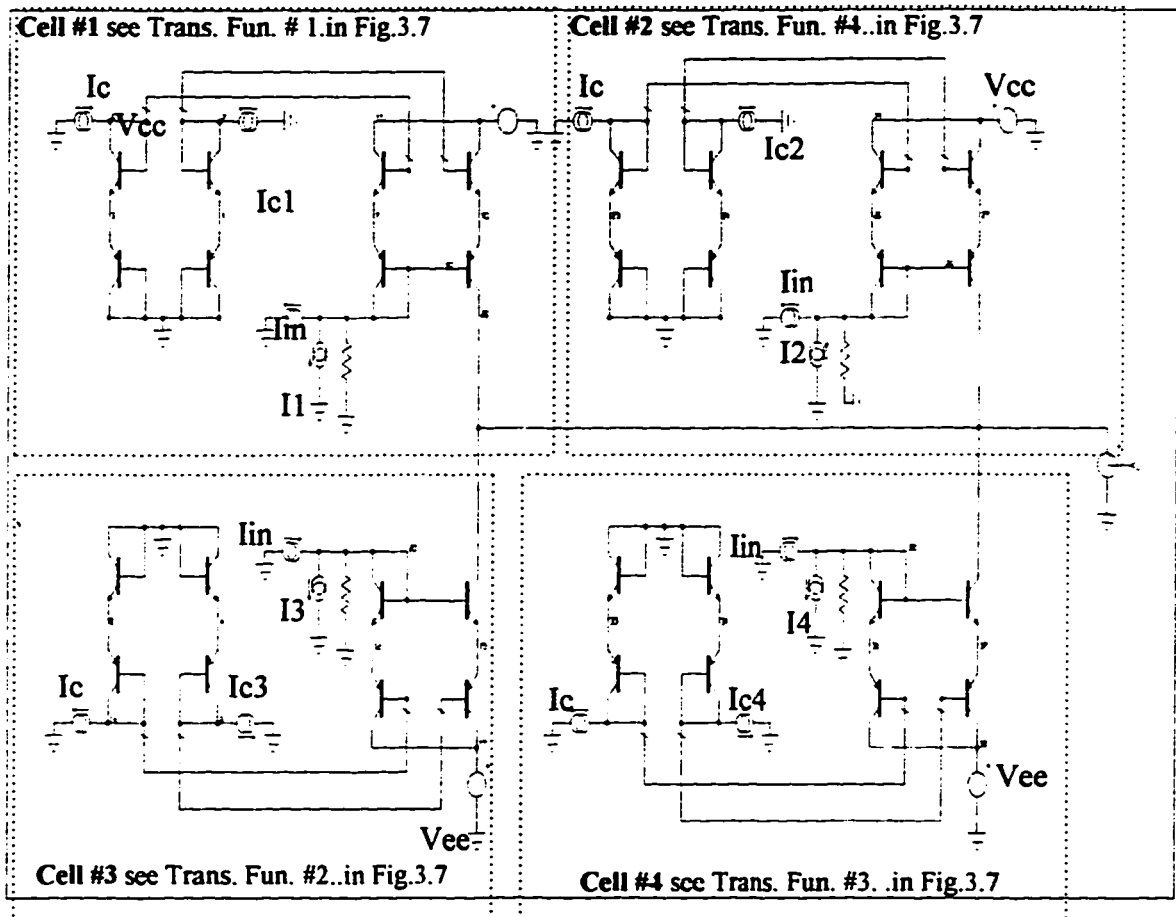
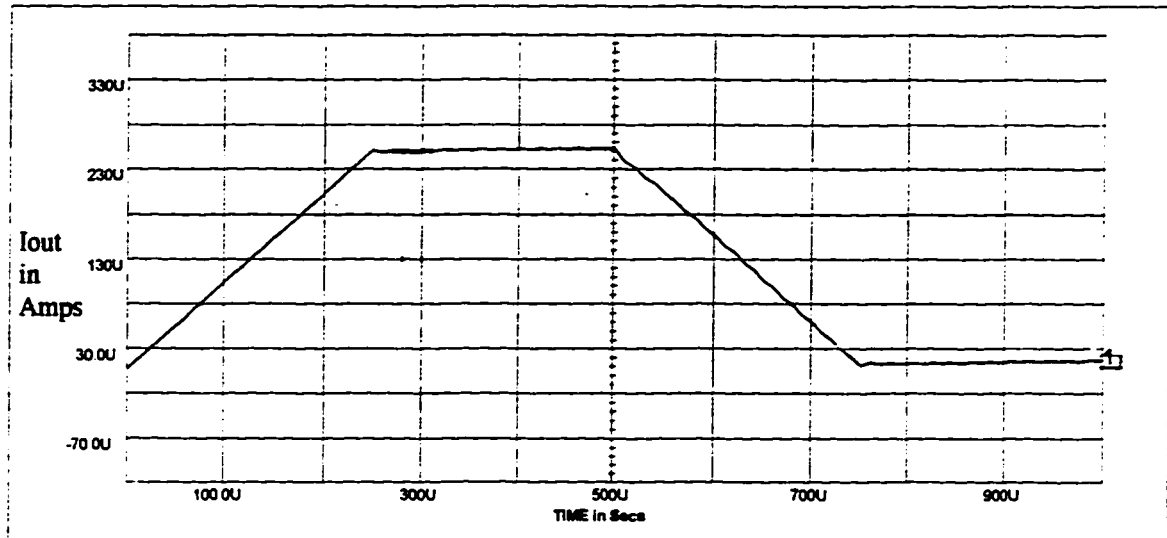


Fig 3.6. a) Circuit implementation of a negative programmable current mirror  
b) Symbol of the circuit  
c) Programmable linear characteristics of the PCM block

In order to understand the circuit in Figure 3.7, used to obtain the trapezoidal function, first notice that this Figure is linked to Figure 3.5. The circuit is divided into four blocks similar to the circuit shown in Fig. 3.6. These blocks, or cells, produce the transfer functions shown in Fig 3.5 with every block associated with its special transfer function. In this way, when all outputs are added together, the trapezoidal function is obtained.



**Fig 3.7** Circuit used to implement the trapezoidal function.(current sources are built from current mirrors.).  $I_1 = 0\text{mA}$   $I_2 = 0.75\text{mA}$   $I_3 = 0.25\text{mA}$   $I_4 = 0.5\text{mA}$  are offset currents  $I_c = 1\text{mA}$ ,  $I_1 = I_c = I_3 = I_4 = 1\text{mA}$  are control currents to obtain different slopes.  $V_{cc} = 5\text{V}$  and  $V_{ee} = -5\text{V}$  are power supply voltages.



**Fig 3.8.** Output simulation result for the circuit implementing the trapezoidal function.

The circuit design approach followed in this section to obtain piecewise linear function approximation is much simpler than the one presented in [34] although they are both based on the use of PGCMs to obtain the desired nonlinear transfer function. In [34], four building blocks were suggested to implement the required function, while only one block is needed in our presented method. In addition to simplicity and fast frequency response, due to the use of current mirrors only, the circuit is temperature independent. This is contrary to the circuit presented in [30] which uses OTAs for the same purpose. Also, the circuit presented in this section is linearly programmable over a wider range. However, it is only suitable for current mode circuits because of its nonzero input impedances. OTAs, on the other hand, can be configured to provide much smaller input impedances.

## **CHAPTER 4**

# **EXPONENTIATING CIRCUITS USING PGCMS**

### **4.1 INTRODUCTION**

The following applications are all based on nonlinear programmable current mirrors. This kind of PCMs is similar to the linear one except that some modifications are added to the control circuit. With these changes, the gain of the PCM becomes exponential. This feature, as will be shown later, is very useful in many nonlinear applications. To start with, exponentiating circuits are presented first.

### **4.2 EXPONENTIATING CIRCUITS**

Arbitrary power-law devices find applications in communication electronics and measurement systems and in the modeling of devices having nonlinear V-I characteristics .

For example, a squarer and a square rooter together with a low pass filter, acting as an integrator for the squarer output, make an excellent root-mean-square (rms) meter.

In this section, some exponentiating circuits will be presented. The work is subdivided into three categories. In two of these, the circuits developed can provide one single output only, while in the other one, multiple outputs with different exponents can be obtained at the same time. For single output circuits, high power exponents can be provided with relatively, compared to a recently published method [31], very low number of components. However, this suggested technique can provide exponentiation only with exponents greater than one. On the other hand, another circuit is given, that can produce exponents less than one only. In all these circuits, the exponent is always a fixed number. To obtain a time varying exponent, a new circuit block diagram, based on the first category, is suggested.

## **4.2.1 SINGLE OUTPUT CIRCUITS**

### **4.2.1.1 HIGH POWER EXPONENTIATING CIRCUITS**

A general method for obtaining an exponentiating circuit is shown in Figure.4.1. Control voltages of the previously explained PCM cell,  $V_{c1}$  and  $V_{c2}$ , are multiplied with another constant and then connected to the main current mirror. Since these two voltages are in logarithmic form of the control currents, after multiplication they become:

$$V_{c1} = V_T * \ln\left(\frac{I_1}{I_s}\right) * E$$

$$V_{c2} = V_T * \ln\left(\frac{I_2}{I_s}\right) * E$$

where E is the desired exponent. Also, since the gain is equal to:

$$\text{Gain} = \text{Exp} [(V_{c1} - V_{c2}) / V_T]$$

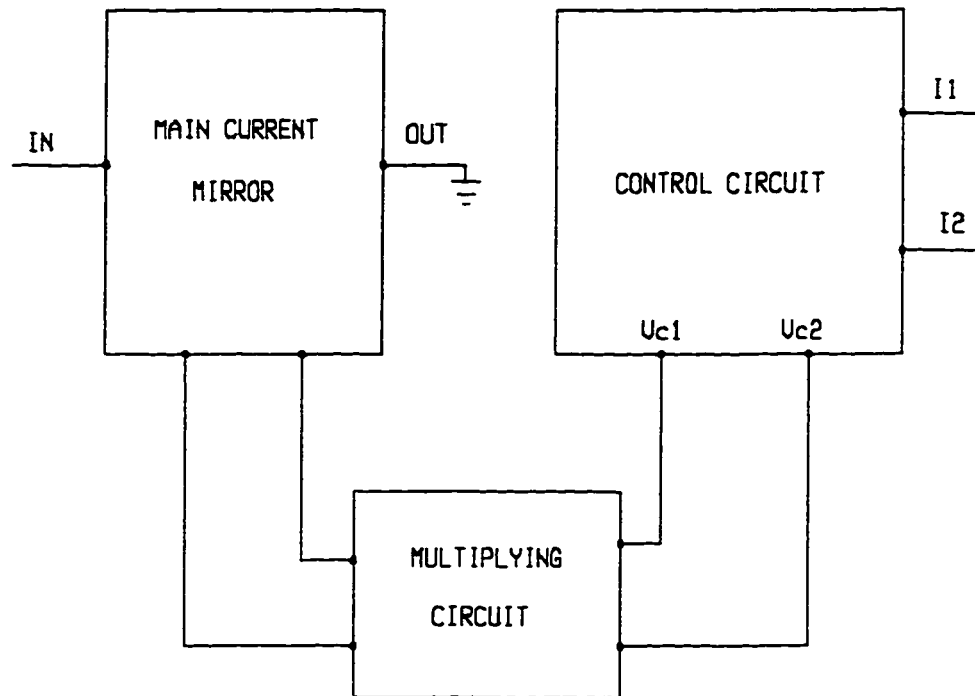
then, after substitution of  $V_{c1}$  and  $V_{c2}$  we get

$$\text{Gain} = \left(\frac{I_1}{I_2}\right)^E$$

$$\Rightarrow I_{OUT} = \left(\frac{I_1}{I_2}\right)^E * I_{IN}$$

By interchanging  $I_{IN}$  with  $I_1$ , the input output relationship will be exponential with E as an exponent. That is

$$I_{OUT} = \left(\frac{I_{IN}}{I_2}\right)^E * I_1 \quad (4.1)$$



**Note:** Full circuit details of every block is provided in the Figure 4.2

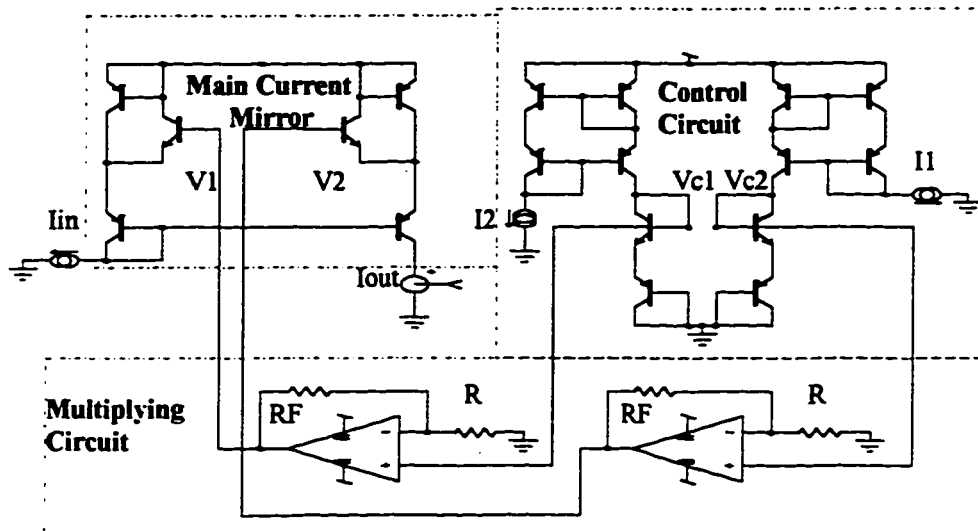
**Fig 4.1.** General method of obtaining an exponentiating circuit.

The multiplication of control voltages with  $E$  can be done in several ways. If the exponent,  $E$ , is time varying, then two four quadrant voltage multipliers are needed. One voltage signal, representing the exponent, must be multiplied with both control voltages. However, if the exponent is a fixed number, whether integer or fractional, then simpler schemes can be applied. One way, shown in Figure.4.2, is to use two OP AMPs, connected in the noninverting mode, in order to perform the multiplication operation. This means that the exponent  $E$  will be of the form:

$$E = 1 + \frac{R_F}{R} \quad (4.2)$$

Which is greater than or equal to one.

Notice that resistors ratios are more important than their values which gives a range for their tolerance. This is useful for monolithic implementations [ 54 ].



$I_{in}=0.1\text{mA}$   $I_2=1\text{mA}$   $I_1=2(1-t)\text{mA}$  for power=4 and  $I_1=(1-t)\text{mA}$  for power of 20. ( $t$  is

Fig 4.2. An exponentiating circuit built from two OP AMPs and one PGCM.

Although simple, this method is more accurate and powerful than a recently published work in [41]. In this published work, the number of OTAs to be used in order to obtain a certain  $E$  is equal to  $4 \times E$ , where  $E$  is a constant. This implies that this method is suitable only for low exponent-power circuits. If high exponents are needed then extensively large circuits must be involved. Moreover, the input of this circuit is temperature dependent and limited in range because of the use of OTAs. In addition, it is impossible to obtain time varying exponents using this method. To show the ability of the



proposed circuit of Figure 4.2 to overcome these disadvantages, an exponentiating circuit with a power of 20 were simulated. In this circuit, only two OP AMPs were used as a multiplying circuit, i.e to multiply control voltages by the required  $E$ , with the programmable current mirror. Simulation results show that the resulting output is in excellent agreement with the expected, mathematically computed output. The error between the two curves was equal to 3% at its maximum. In addition, no extra power supply, more than five volts, was needed. Results are displayed in Figure 4.3 and 4.4.

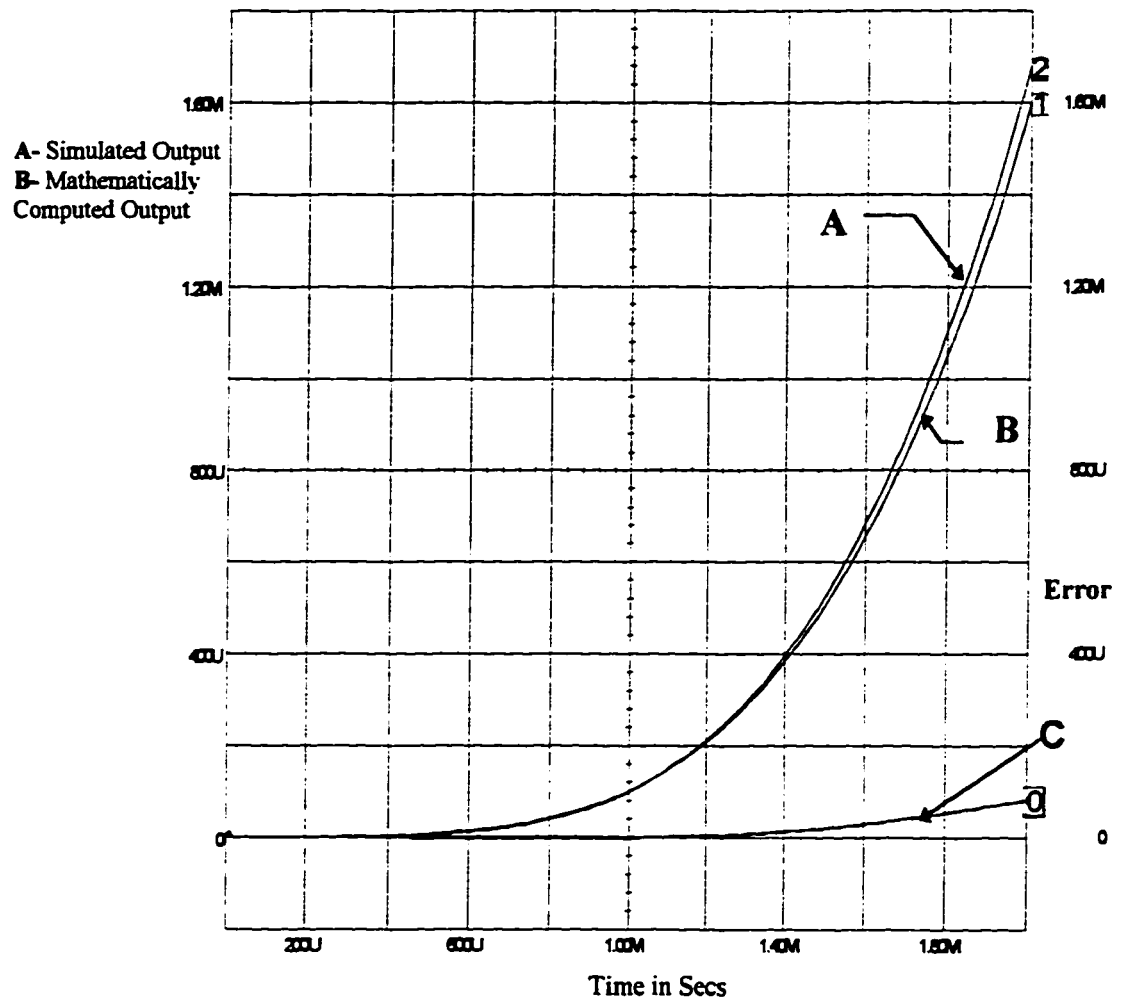


Fig 4.3. Simulation result of the exponentiating circuit implementing the function  $I_{OUT} = I_{IN}^2$ .

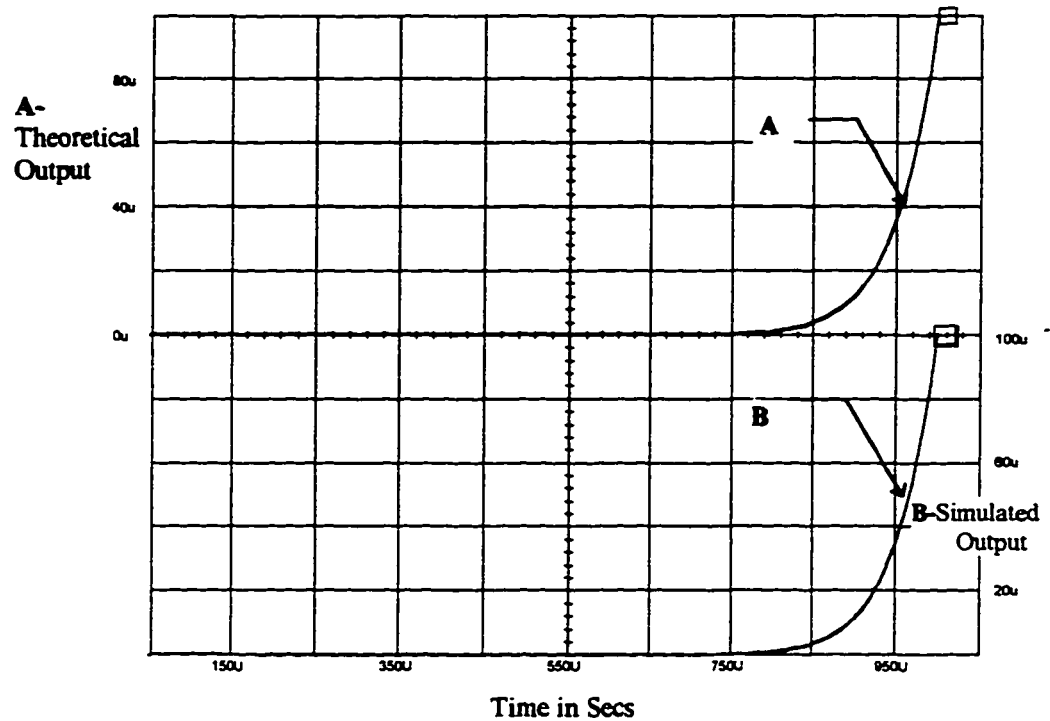
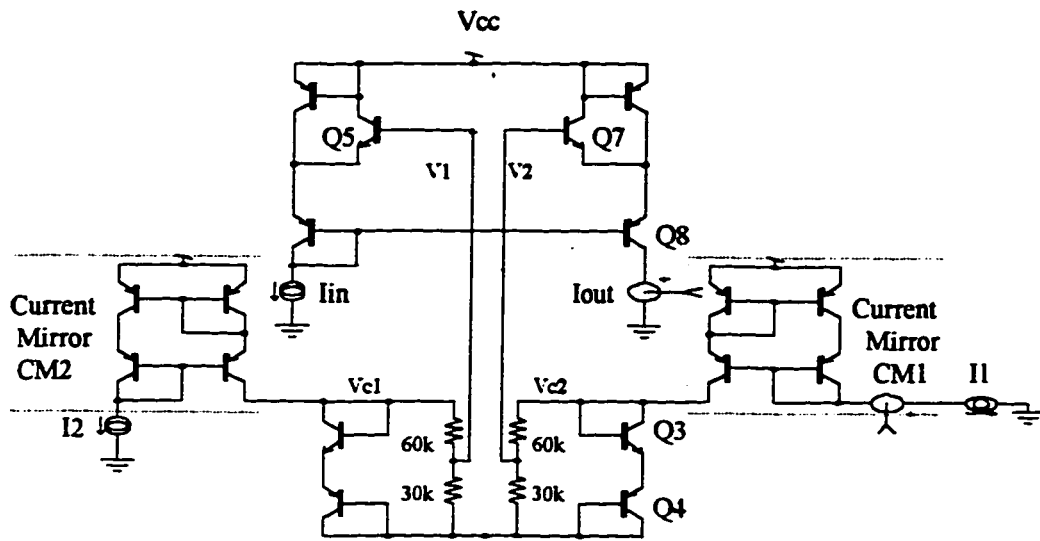


Fig 4.4. Simulation result of the exponentiating circuit implementing the function  $I_{OUT} = I_{IN}^{20}$ .

#### 4.2.1.2- EXPONENTIATION WITH SMALL EXPONENTS

**4.2.1.2.1- Using Potentiometers.** For small exponents that are less than one, or larger than one but still not too large, the previous circuit is considered to be area consuming because of the use of two Op Amps. For these reasons, other exponentiating circuits were developed. However, the same methodology used to obtain the previous circuit is followed here. Instead of using two OP AMPs to perform multiplication, two potentiometers can be used to divide the control voltages by some fraction and then

resulting voltages are fed to the main cell. This will provide exponents that are only less than one. As an example, the cubic root circuit of Figure.4.5. was simulated using ICAPS. In this circuit, CM1 and CM2 current mirrors are used to pump  $I_2$  and  $I_1$  into diode connected transistors  $Q_1$  - $Q_2$  and  $Q_3$  - $Q_4$  respectively to produce  $V_{c1}$  and  $V_{c2}$ . These two voltages are divided using the  $30K\Omega$  and  $60K\Omega$  resistors to obtain  $V_1$  and  $V_2$ . This is equivalent to multiplying the control voltages  $V_{c1}$  and  $V_{c2}$  by  $1/3$ . Thus, when the two voltages  $V_1$  and  $V_2$  are fed to the main current mirror composed of  $Q_5$  - $Q_8$ , a cubic root circuit is obtained.  $Q_5$  and  $Q_7$  transistors are of Darlington type which possesses a large beta value. This type was used in order not to have any loading effect on  $V_1$  and  $V_2$  from the main mirror circuit. Also the potentiometer resistor values are chosen large in order not to affect the two voltages  $V_{c1}$  and  $V_{c2}$  across the diode connected transistors. These resistors are of  $30k\Omega$  and  $60k\Omega$  value. The output of this circuit is shown plotted in Figure.4.6. Resulting output has a maximum error of 1.7% which is considered very precise.



$I_2 = 1\text{mA}$   $I_{in} = 100\mu\text{A}$   $I_1 = (1-t)\text{mA}$ . Where  $t$  is the time.

Fig 4.5. Cubic root circuit.

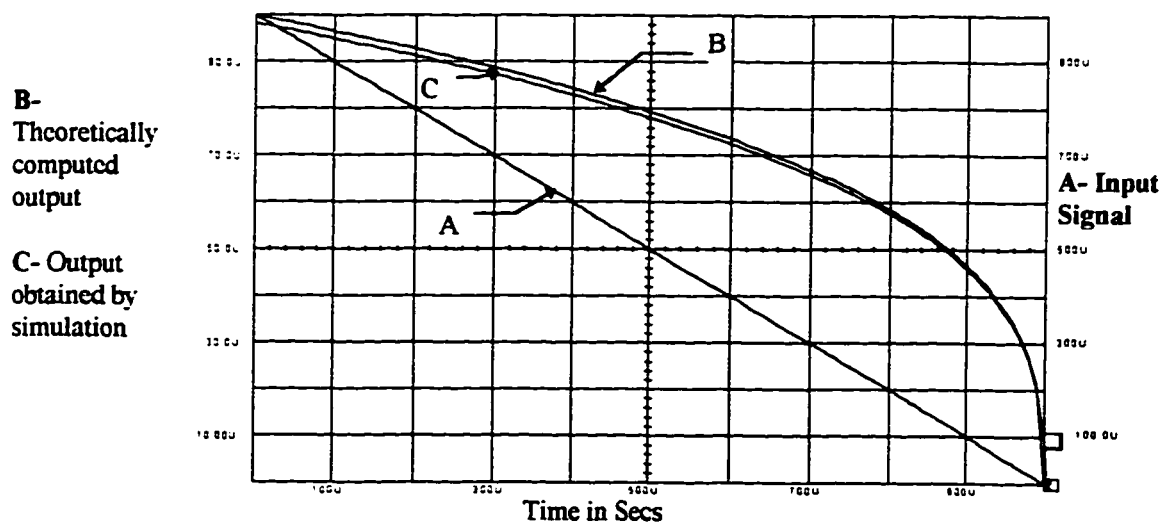


Fig 4.6. Simulated output of cubic root circuit.

**4.2.1.2.2 Using Additional Diodes** Inserting some diodes in the main and control parts of the PCM cell yields another simple exponentiating circuit. To illustrate this point, consider the circuit shown in Figure 4.7, where N diodes are added to the control circuit and other M diodes are added to the main one. This changes the control voltages and the gain of the cell to

$$V_{C1} = V_T * \ln \left( \frac{I_{IN}}{I_S} \right) * N$$

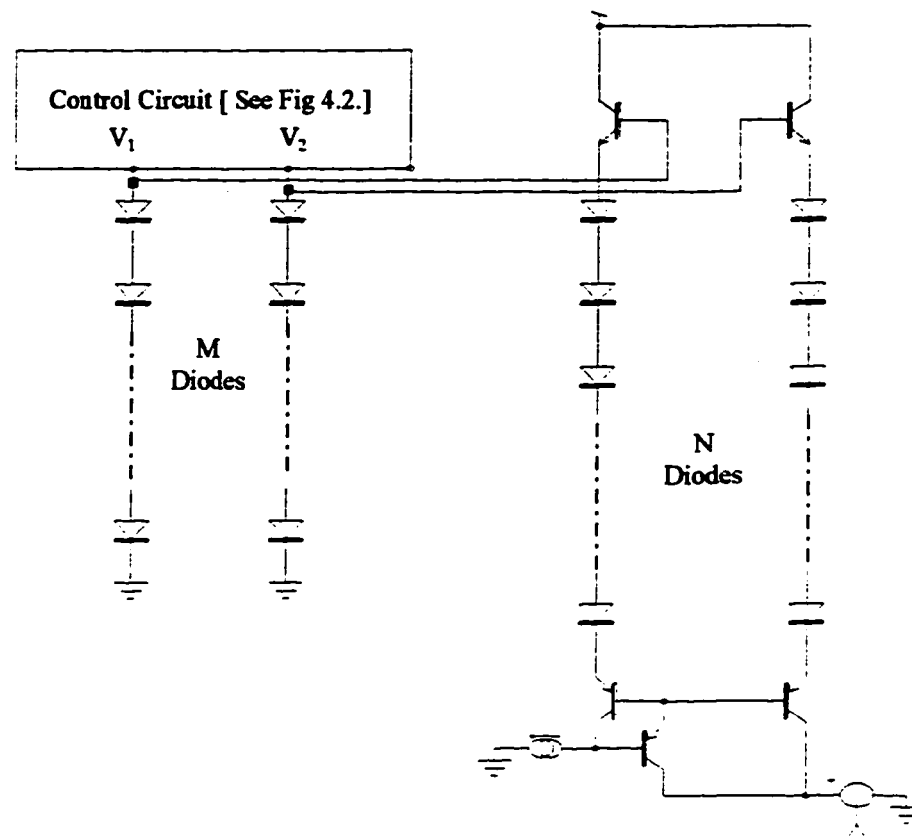
$$V_{C2} = V_T * \ln \left( \frac{I_2}{I_S} \right) * N$$

By doing KVL around the loop of transistors Q1-Q4, the following relation for the gain can be easily obtained :

$$\text{Gain} = \text{Exp} [(V_{C1} - V_{C2}) / (M * V_T)] = \left( \frac{I_{IN}}{I_2} \right)^{N/M}$$

So,

$$I_{OUT} = \left( \frac{I_{IN}}{I_2} \right)^{N/M} * I_1 \quad (4.3)$$



**Fig 4.7.** Circuit used to obtain rational exponents by adding diodes.

Using this method, a linear input signal was squared. Circuit diagram and resulting output are shown in Figure. 4.8 and 4.9 respectively, where the input,  $I_N$  was chosen to be sinusoidal with frequency of 1KHz. The two current mirrors, CM1 and CM2 are used to rectify the input current before feeding it to the diodes network to obtain  $V_{c1}$  and  $V_{c2}$ . Notice that these mirrors are biased only using the input current and not through any other DC. This must be assured in order to square the input signal alone without any additional biasing current. Transistors  $Q_1$  and  $Q_2$  are used as input buffers to supply the two mirrors with  $I_1$ . A better method is to use the class AB circuit that was used in Figure 2.5 to implement the MOPCC. This will avoid any crossover distortion because  $Q_1$  and  $Q_2$  will be biased and ready to conduct small current values of  $I_1$ . Similarly  $I_2$ , a DC current, is fed to the diodes network via CM3. Also, an additional DC current has to be added to the output of the circuit in order to reduce any current offset produced by the circuit due to transistors mismatch or to the differences between PNP and NPN transistors.

The output spectrum shows an error in the amplitude of the resulting current which is due to the inaccuracy of the used mirrors, specially CM3. Although the crossover distortion is not apparent in the spectrum of the output, this could be because it is very close to the main frequency component. This method is useful if the exponent can be written as a ratio of two integers. However, if this is impossible, the only alternative is to use OP AMPs or potentiometers.



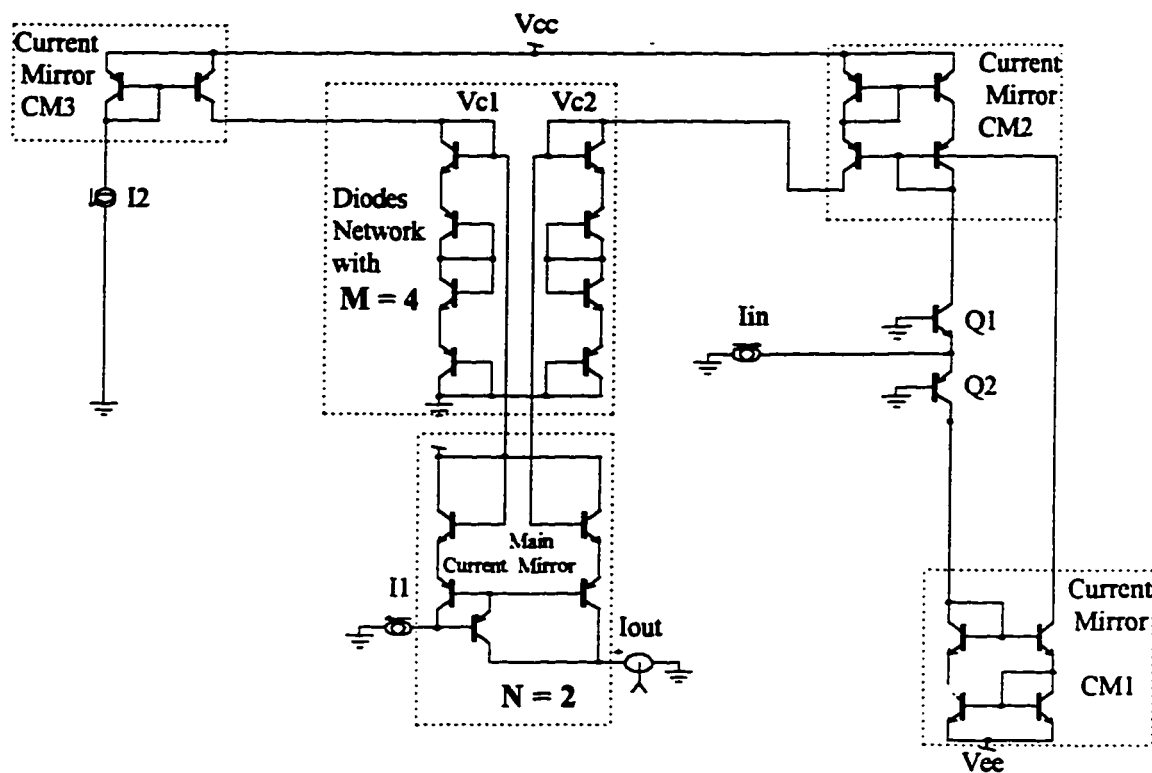


Fig 4.8. Squaring circuit. ( $I_2 = 10\text{mA}$   $I_{in} = 10\text{m sin}(\omega t)$   $I_1 = 1\text{mA}$   $V_{cc} = -V_{ee} = 5\text{V}$ ).

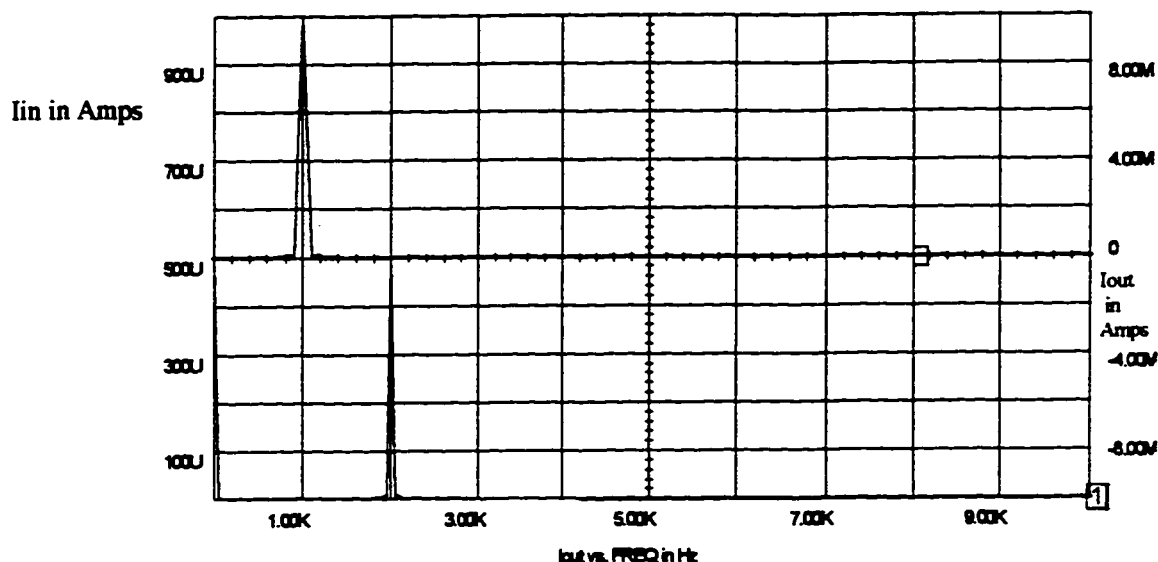


Fig 4.9. Amplitude spectrum of squaring circuit output when driven by a sinusoidal signal with frequency of 1KHz.

**4.2.1.2.4 Comparison with Others Realisations** This section includes a comparison between the last two circuits and the ones obtained by other researchers. To start with, the difference between functions of the two circuits must be made clear. The main difference is that the circuit in Figure 4.5, which uses potentiometers to control the exponent value, provides exponents that need not be expressed as a ratio of two integers while the one in Figure 4.8 doesn't do so. In applications where the exponent can be expressed as a ratio of two integers, as was shown in the second circuit, using diodes to obtain  $E$  is much preferable because of the better accuracy that can be obtained and the suitability for integration on a chip. The reason of the low accuracy in the circuit that uses potentiometers is that these are normally adjusted manually. Also, as mentioned earlier, these resistors must be set at large values which means that they will occupy a large area

on the chip and will dissipate a large amount of power. In so many applications this is not accepted. Moreover, these resistors are difficult to simulate because of the same reason.

Power law circuits are already available in so many publications, [24-32 ]. These are built using multipliers, OTAs, CMOS transistors operating in their saturation or subthreshold modes, BJTs using the translinear principle or MOSFETs with operational amplifiers or with current conveyors. In order to compare such a group of circuits with the proposed circuits, it is better to outline the important features on which this comparison will be based. These are: simplicity, accuracy, temperature independence, area occupancy, possibility to increase number of inputs and outputs, modularity and programmability, and finally frequency performance.

The proposed circuits are superior than those mentioned in the above references in terms of modularity and programmability. Only the circuit in [30] owns this feature. However, in this circuit, all other features are either not available or are less than those in the proposed circuits. Disadvantages of the circuit in [30] were discussed in section 4.2.1.1. Because our circuit belongs to the family of translinear circuits, it is temperature independent and possesses a good frequency response. The last feature is true also because the circuit operates in current mode.

Compared with the others, it is clear that proposed circuits are not good regarding their area occupancy. Although the circuit in Figure 4.8 consumes much less area than

the one in Figure 4.5, still it is considered large when the value of the exponent,  $E$ , is low. It is true that the higher the value of  $E$  is, the larger the circuit will become, but the circuit growth, with the increase of  $E$ , is much lower than most of the others. There are some circuits which use only few MOS transistors to construct squaring and cubing circuits, [27, 28]. These transistors are by themselves small compared to BJTs which constitute the proposed circuits. Finally, the circuits are similar in terms of simplicity, which means the design procedure of the circuit, and accuracy to their counterparts that are based on the use of transistors only [24 -28]. Those are mostly built using the translinear principle or are based on square law characteristics of MOSFETs.

## 4.2.2 MULTI OUTPUT EXPONENTIATION CIRCUITS

To obtain more than one output, with different exponents, from the same circuit, more control voltages are required, two for each output. These control voltages will be fed to their corresponding mirrors. Exponents of 1, 2, 3,.....etc., can be generated at the same time by stacking two diodes, in the control circuit, for each exponent. This kind of circuits will be very useful for geometrical functions approximation as will be shown in chapter 5. The main drawback of this technique is that the more the number of required outputs is, the lower the accuracy of high exponent outputs becomes. This is because the input current, entering the base emitter junction of input transistor of the mirror, is reduced by

base currents of output transistors for every output. In order to reduce this decrease, transistors in the main circuit which are directly connected to the control voltages must have large  $\beta$  values in order to minimize their base currents. This is easily achievable by using composite bipolars. An additional feature provided from such a topology, is that one can obtain more than one output, of the same power, but with different weights,  $I_{NM}$ 's, as shown in Figure.4.11. Since this circuit is going to be used in some other, more important, applications ,it's analysis and testing will be discussed in chapter 5.

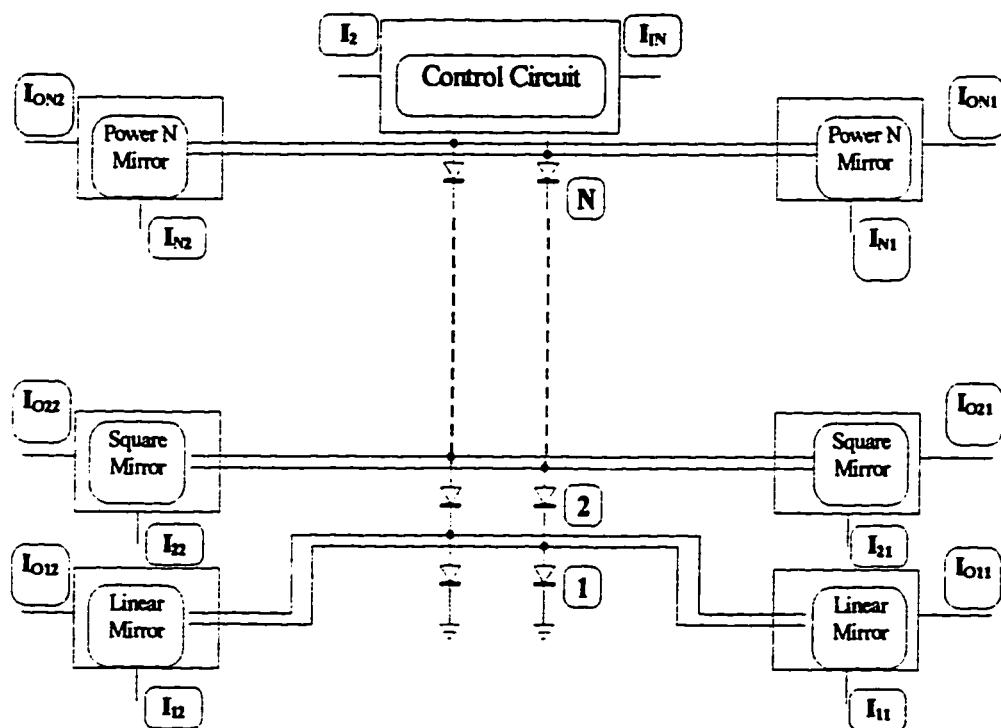


Fig 4.10. Multi output exponentiating circuit. For details of control and power N circuits, see Fig 4.2.

## CHAPTER 5

# ANALOG FUNCTION SYNTHESIS BASED ON TAYLOR SERIES

### 5.1 BASIC PRINCIPLE

In this section, a new powerful technique for analog functions synthesis is presented. It is based on the previously explained multiple output exponentiating circuit. This circuit is capable of generating all Taylor series terms for any continuous function. By making use of the fact that this circuit can provide different weights for every exponent output, it is possible to synthesize more than one function at the same time. This is achievable if the appropriate terms, associated with the Taylor series expansion of the required functions, are summed together at one point. Of course, it is impossible to sum all Taylor series terms because those are infinite. However, good approximations can be obtained if the series is truncated at some high order term. This is possible because the exponentiating circuit is capable of generating large exponents without additional power

supply, if small currents with the required ratios are used. However, the higher the term is, in Taylor series, the lower its coefficient becomes. Unfortunately, the exponentiating circuit can not provide very small and precise weights. In order to overcome this problem, without adding any new components, the diodes network, connected to the control circuit, has to be changed. Simply, diodes areas should be proportional to their rank in the diodes network. For more clarification, see Figure 5.1. Following this method, control voltages for the Nth power mirror become:

$$\begin{aligned}
 V_{c1} - V_{c2} &= V_T \cdot \ln\left(\frac{I_N}{N \cdot I_s} \cdot \frac{I_s}{I_2}\right) + V_T \cdot \ln\left(\frac{I_N}{(N-1) \cdot I_s} \cdot \frac{I_s}{I_2}\right) + \dots \\
 &+ V_T \cdot \ln\left(\frac{I_N}{1 \cdot I_s} \cdot \frac{I_s}{I_2}\right) \\
 &= V_T \cdot \ln\left(\frac{I_N}{N! \cdot I_2}\right)^N
 \end{aligned}$$

This implies that the gain will be

$$\text{Gain} = \exp\left(\frac{V_{c1} - V_{c2}}{V_T}\right) = \left(\frac{I_N}{N! \cdot I_2}\right)^N$$

Thus, the *Nth* output becomes:

$$I_{OUT} = I_1 \cdot \left(\frac{I_N}{N! \cdot I_2}\right)^N \quad (5.1)$$

Which is in the form of a Taylor series term.

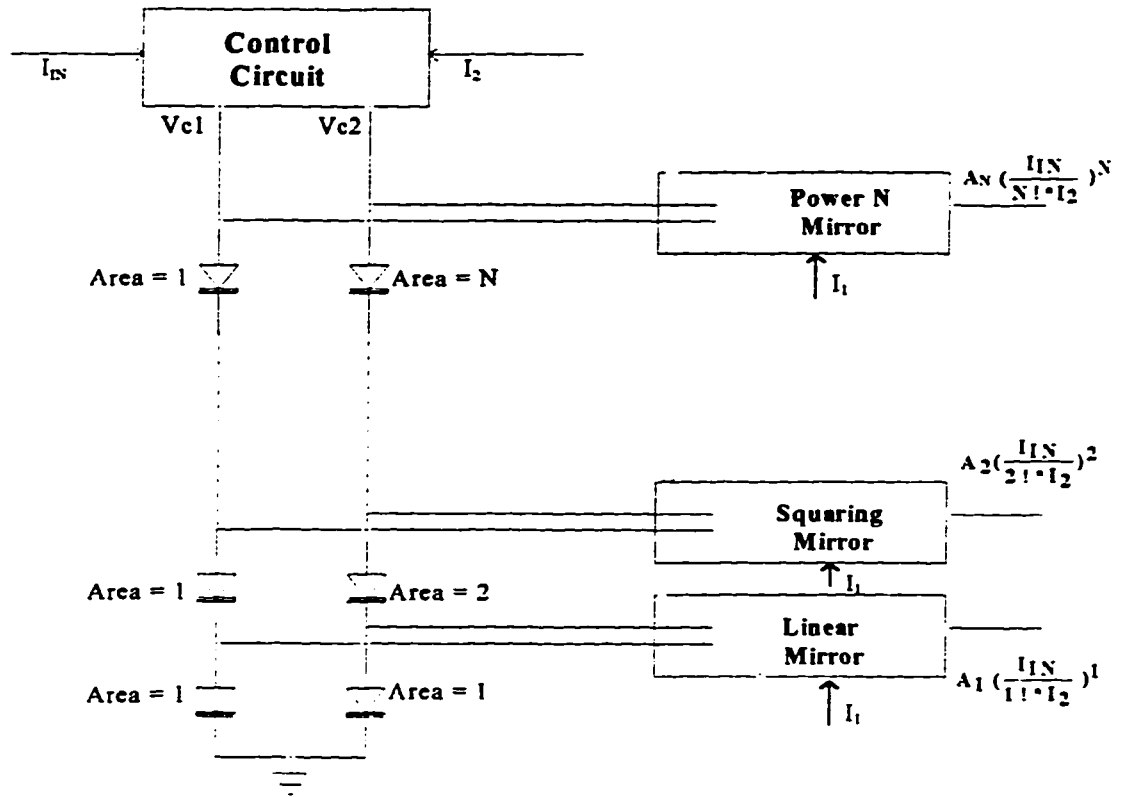


Fig 5.1. General description of circuit used to obtain Taylor series terms.

Although simple, this method is very powerful in synthesizing any function using Taylor series. Moreover, since the circuit is capable of providing different weights for every term of the series, one can synthesize more than one function at the same time. All circuits published in the literature do not have this feature [ 25,33,34,37,38, 40-42 ]. They are designed mainly to implement only one single function and can not be



programmed to synthesize other functions. Also, this circuit can be easily integrated using MOS transistors, operating in their sub threshold region, which reduces its power consumption. This shows the versatility of the suggested circuit and makes it very suitable for future analog electronic systems. To support these claims, the following examples are given.

## 5.2- EXAMPLES

### 5.2.1 SYNTHESIS OF THE BESSEL FUNCTION

The Bessel function is very well known mathematically. It is widely used in so many applications specially in communications. Until now, no circuit capable of implementing this function was published in the literature. This is mainly because of its complicated mathematical expression. However, the following expansions can be used see [43 ].

$$J_n(m) = \left(\frac{m}{2}\right)^n \left[ \frac{1}{n!} - \frac{\left(\frac{m}{2}\right)^2}{1! * (n+1)!} + \frac{\left(\frac{m}{2}\right)^4}{2! * (n+2)!} - \frac{\left(\frac{m}{2}\right)^6}{3! * (n+3)!} + \dots \right]$$

Thus for order 0, it becomes

$$J_0(m) = 1 - \left(\frac{m}{2}\right)^2 + \frac{\left(\frac{m}{2}\right)^4}{2! \cdot 2!} - \frac{\left(\frac{m}{2}\right)^6}{3! \cdot 3!} + \dots$$

$$\Rightarrow J_0(m) = 1 - \left(\frac{m}{2}\right)^2 + \frac{\left(\frac{m}{2}\right)^4}{4!} - 20 \cdot \frac{\left(\frac{m}{2}\right)^6}{6!} + \dots \quad (5.2)$$

Which is in the form of Taylor expansion.

Similarly,

$$J_1(m) = \left(\frac{m}{2}\right) - \frac{\left(\frac{m}{2}\right)^3}{1! \cdot 2!} + \frac{\left(\frac{m}{2}\right)^5}{2! \cdot 3!} - \frac{\left(\frac{m}{2}\right)^7}{3! \cdot 4!} + \dots$$

$$\Rightarrow J_1(m) = \left(\frac{m}{2}\right) - 3 \cdot \frac{\left(\frac{m}{2}\right)^3}{3!} + 10 \cdot \frac{\left(\frac{m}{2}\right)^5}{5!} - 35 \cdot \frac{\left(\frac{m}{2}\right)^7}{7!} + \dots \quad (5.3)$$

In order to implement these functions, the only thing required is to program the circuit with the required coefficients. These are: -1, 1, 20 and 1, -3, 10, -35 for the two functions respectively. Notice that when the function is odd, mirrors generating even powers are redundant and vice versa. Negative coefficients can be obtained by mirroring the output of the corresponding term, before summing it with the others to produce the final output. Notice that only those terms appearing in equations 1 and 2 were implemented. This will make the synthesized output valid only in the following range:

For  $J_0$  &  $J_1$ , range of  $m$  is:  $-3 < m < 3$ . ( With an error of 11% and 7% respectively.)

Finally, for  $J_{0,,}$  a DC component of 1 mA must be added. However, the required current may be less than that because of the resulting DC offset of the circuit. This current should be adjusted such that the function becomes zero at the appropriate values of  $m$ . Figure 5.2 shows a simplified schematic of the full circuit used to obtain both functions. In this circuit, all transistors have the same area and are identical. Only transistors used in main mirrors have to be matched. Since the desired exponents are 1, 3, 5 and 7 control voltages were obtained from the first two, six, ten and fourteen diode connected transistors. Notice that two diode networks are used together with bipolar main mirrors. This is done to accept positive and negative input signals.

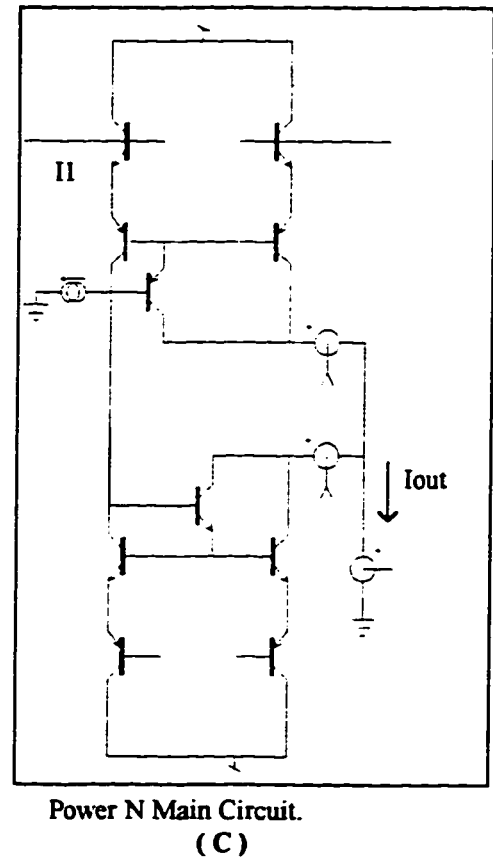
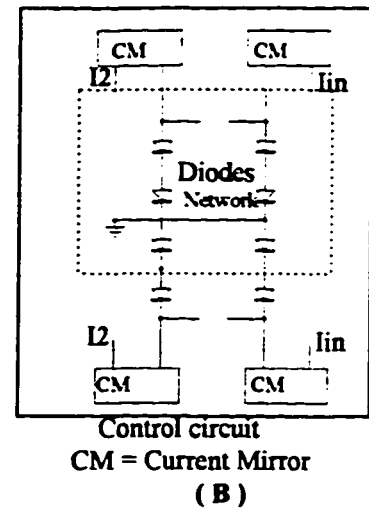
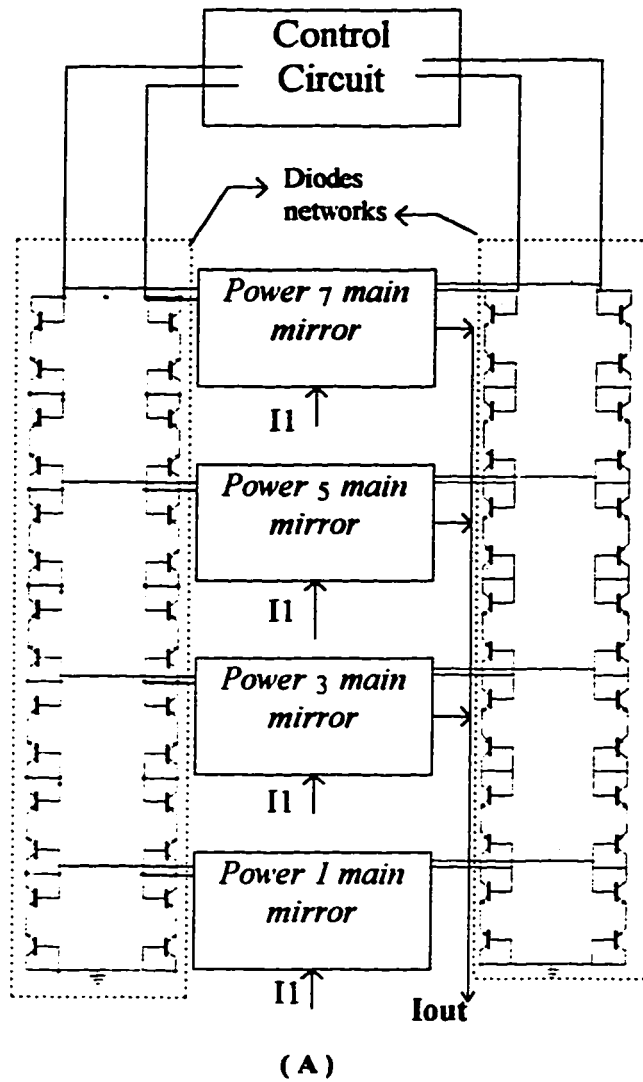


Fig 5.2. Circuit used to synthesize Bessel and Sine functions.

A) Main circuit ( simplified )

B) Control circuit (simplified )

C) Power N main circuit

Simulation results for both Bessel functions are shown in Figure 5.3 and 5.4. A maximum error of 15% and 11% ,with respect to the maximum of the Bessel function, was obtained for J0 and J1 respectively. This maximum happens when the input current reaches its maximum, i.e. 3mA. These Figures are very close from the expected error of truncation. The main reason for this high accuracy is the use of transistors with  $\beta = 10000$ .

Transistors used for simulation are 2N2222, an NPN transistor, and 2N2905, a PNP transistor.

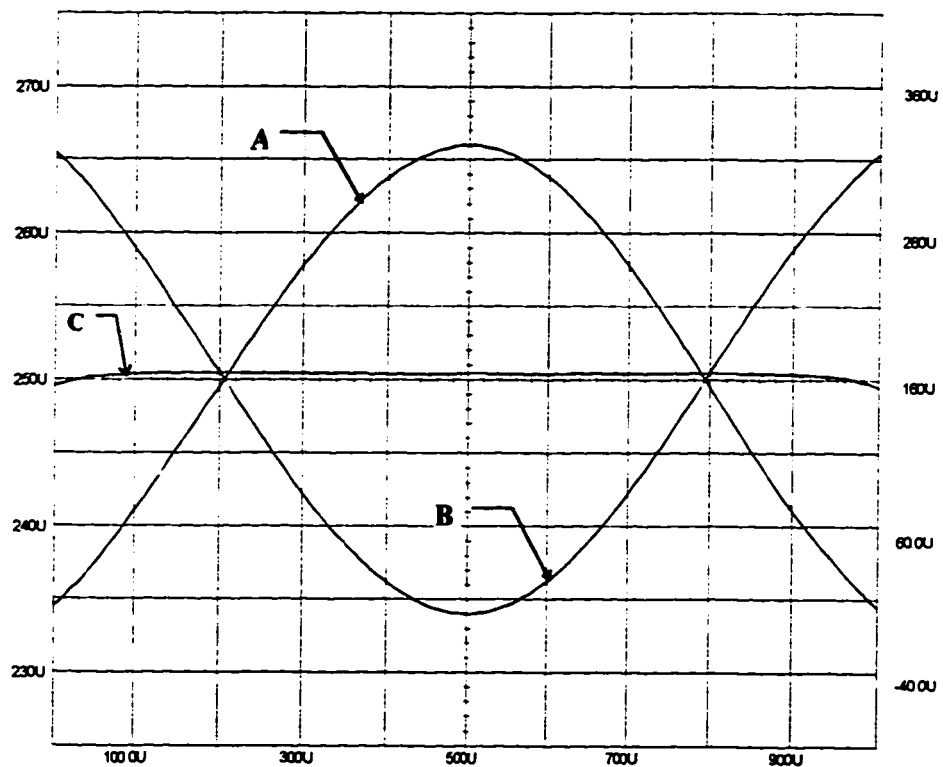
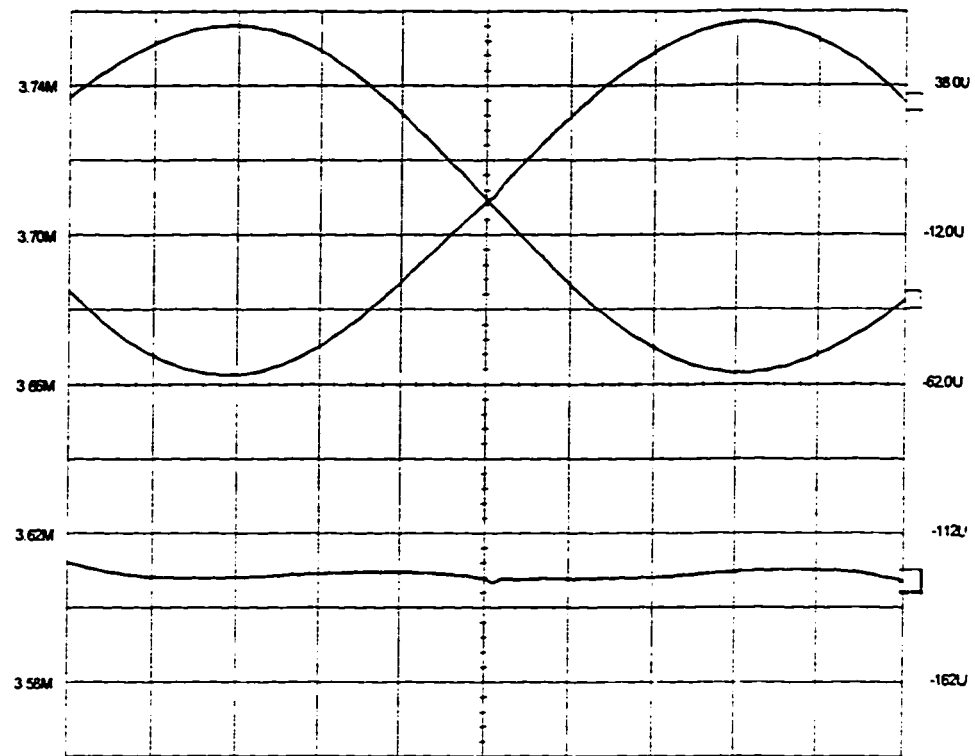


Fig 5.3. Comparison between computed and simulated Bessel function with order 0.

- A- Mathematically computed Bessel function
- B- Inverted output obtained by simulation
- C- Difference between A and B



**Fig 5.4.** Comparison between computed and simulated curves of Bessel function with order 1.

*A- Mathematically computed Bessel function*

*B- Inverted output obtained by simulation*

*C- Difference between A and B*

## 5.2.2 SYNTHESIS OF THE SINE FUNCTION

Following the same procedure used to obtain the Bessel function, Sine function can be synthesized too. No extra hardware is needed if only one output is required. However, the circuit can be extended to provide outputs of both functions, Sine and Bessel, at the

same time. This will be at the expense of extra current mirrors to be connected to the same control circuit. The number of these additional mirrors is equal to the number of terms needed to approximate the Sine function. An additional requirement, for obtaining multi outputs, is to increase  $\beta$  values for transistors connecting every current mirror to its corresponding control voltages. As mentioned earlier, composite bipolar transistors, shown in Figure 5.5, are more than adequate for this purpose. As a first step, the sine function is expressed as

$$\sin(x) = \alpha_1 x - \alpha_2 \frac{x^3}{3!} + \alpha_3 \frac{x^5}{5!} - \alpha_4 \frac{x^7}{7!} + \dots \quad [5.4]$$

Where  $\alpha_n = 1$  for all  $n > 0$

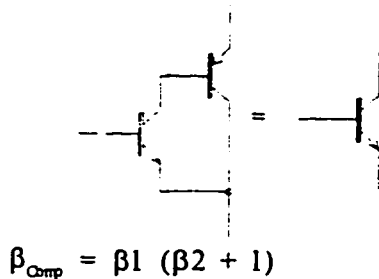


Fig 5.5 Composite bipolar transistors

This means that the coefficients,  $\alpha_n$ , of all terms are equal in magnitude. Those are represented by input currents to the different mirrors composing the circuit. Hence all

those currents are set equal. Using only the first four terms of the Taylor expansion, the input range becomes:  $-3 < X < 3$  with an error of 5.5 % for the output. Simulation results, using the same input current for the previous circuit, are shown in Figure 5.6. A maximum error of 8% is obtained when  $I_{in} = 3\text{mA}$ . This is also very close from the theoretically expected error, 5.5%. Notice that  $I_2$  must be set to  $1\text{mA}$  for this case. Previously, for the Bessel function, it was  $2\text{mA}$  to obtain the divide by 2 factor appearing in equations 1 and 2. Finally, negative weights are obtained by mirroring the output of the corresponding N-power main mirror before summing with other outputs. Figure 5.7 shows that harmonic distortion of the resulting output is almost negligible.

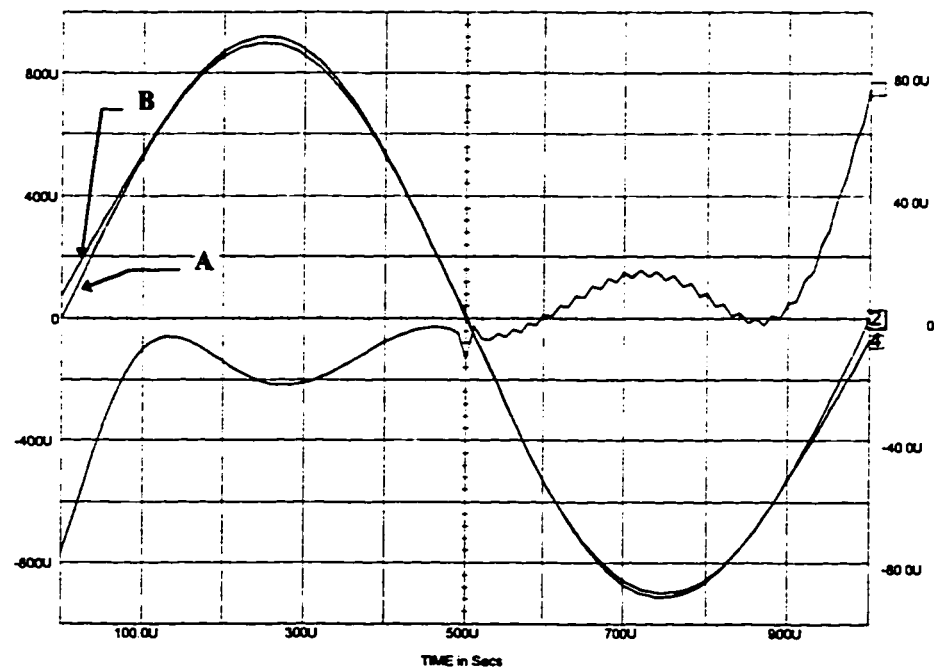


Fig 5.6. Comparison between mathematically computed and simulated sine function.

*A- Mathematically computed Sine function*  
*B- Output obtained by simulation*  
*C- Difference between A and B*



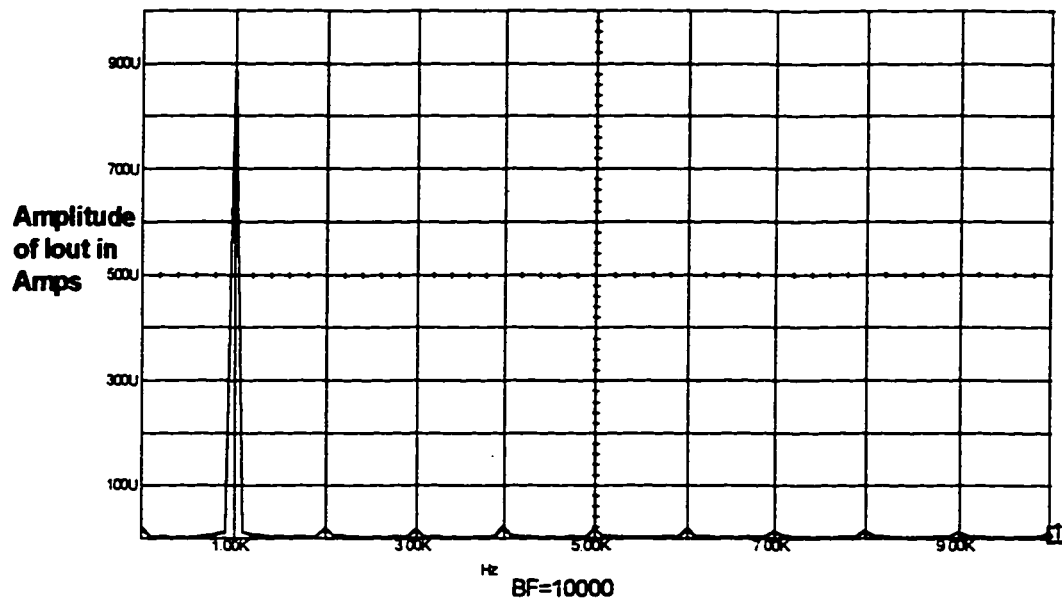


Fig 5.7. Frequency spectrum of the sine circuit output.

### 5.3 COMPARISON WITH OTHERS WORK

In this section, a comparison will be made between the presented electronically programmable analog function synthesizer, or AFS, and previously published circuits. The power of this circuit appears clearly in the last two examples. Although most of the previously published circuits were built to implement only one function, there isn't any circuit, available in the literature, which is capable of implementing the Bissell function even with order zero.

Previous techniques are based on the use of multipliers [29], operational amplifiers and transistors [32], or transistors only [40- 42, 45]. Only the translinear principle provides a mean for implementing a wide range of functions on the transistor level only. This is the least area consuming and the most accurate method. Even though, each function is associated with a different circuit. The AFS belongs to the same category with two exceptions. First, it is electronically programmable. This means that the function to be synthesized can be varied simply by changing few parameters. The second difference is its ability to provide multiple outputs. This is due to the use of nonlinear current mirrors to construct the output. Regardless of these two differences, the circuit can be easily annualized using the translinear principle.

One of the recent works, based on the use of the translinear principle to implement different analog functions, is found in [44 ]. In this work, the author suggests a method for approximating all geometric functions using simple rational expressions. These are then implemented using the translinear principle. The same method can be used to approximate nongeometric functions too. Resulting circuits are smaller in area than the AFS. However, they are single output and nonprogrammable. Both circuits are fast in their response and temperature independent. This is because they are current mode circuits built using the translinear principle.

The input range of all circuits in [44] is fixed and associated with a certain accuracy that can't be increased. However, for the AFS, the input range can be increased if higher terms of the Taylor series expansion are implemented. On the other hand, as the number of high order terms that are implemented is increased, as the accuracy of the final output increases. This is true only if the input range is kept constant. Thus if higher accuracy is wanted, the circuit area must be increased.

One more difference is that the suggested AFS is built using BJT transistors only. MOSFETs can be used only for low power, low frequency applications [1]. However, the circuits in [44] can be implemented using BJTs or MOSFETs but not both. This is because the translinear principle itself was generalized for both transistor types [25]. Finally, there is no fixed step by step method for implementing the functions presented in [44]. In contrast, The AFS is based on Taylor series expansion which is very well known. Also, the implementation method is very simple and clear.

## CHAPTER 6

# FREQUENCY MULTIPLICATION USING NONLINEAR PGCMS

### 6.1 INTRODUCTION AND MATHEMATICAL BACKGROUND

Another important application of nonlinear circuits is frequency multiplication. Because of its very wide range of applications, many researchers were involved in this subject. Over the past few decades, many frequency doubling and tripling circuits were presented in different publications [46,47]. However, to obtain higher order frequency multiplication, the common technique was to use a multiplying circuit that produces an output having two frequencies equal to the sum and the difference of the two input frequencies. This is followed by a filter to eliminate the unwanted frequency. Another method is to cascade more than one doubler or tripler. Also, nonlinear devices could be used to obtain several multiples of the input frequency plus some other related harmonics.

Unwanted components are then filtered to leave the required output only. No single circuit, to the knowledge of the author, is capable of doing a general, i.e. double, triple ....etc., frequency multiplication operation.

In this section, a new technique, based on nonlinear PGCMs, is introduced. The proposed circuit enables us to perform high order frequency multiplication. The circuit is general, in the sense that it can be programmed to perform any frequency multiplication required subject to the condition that a perfectly precise PGCM exists. Since this is not the case, the highest frequency obtained is 7 times the input signal frequency. In addition, the circuit can be configured to obtain multiple outputs with a different multiplication factor for every output.

In order to implement such a circuit, mathematical foundations must be provided first. The input signal is assumed to be sinusoidal with a radial frequency of  $x$ . This means that the output will be of the same form except that its frequency is  $Nx$ . The circuit to be implemented should be able to manipulate the input signal mathematically until the output is produced. Since the output has a different frequency than its input, the circuit must be nonlinear. Looking at the amplitude spectrum of an output of the exponentiating circuit, we find that it is composed of a number of signals at odd or even multiplicands of the input frequency depending on the exponent. This is explained mathematically by the following relations:

$$\sin^7(x) = \frac{1}{64} [35 \cdot \sin(x) - 21 \cdot \sin(3x) + 7 \cdot \sin(5x) - \sin(7x)]$$

$$\sin^5(x) = \frac{1}{16} [10 \cdot \sin(x) - 5 \cdot \sin(3x) + \sin(5x)]$$

$$\sin^3(x) = \frac{1}{4} [3 \cdot \sin(x) - \sin(3x)]$$

$$\sin^6(x) = \frac{1}{32} [10 - 15 \cdot \cos(2x) + 6 \cdot \cos(4x) - \cos(6x)]$$

$$\sin^4(x) = \frac{1}{8} [3 - 4 \cdot \cos(2x) + \cos(4x)]$$

$$\sin^2(x) = \frac{1}{2} [1 - \cos(2x)]$$

Notice that, when the power is even, the output contains even frequency harmonics and when the power is odd, the output contains odd harmonics. Hence, based on the above equations, the addition of a number of signals representing different odd exponents of the input can lead to the cancellation of all harmonics except the desired one. This can be expressed mathematically by:

$$\sin(7x) = -64 \cdot \sin^7(x) + 112 \cdot \sin^5(x) - 56 \cdot \sin^3(x) + 7 \cdot \sin(x) \quad (6.1)$$

$$\sin(5x) = \frac{1}{4} [64 \cdot \sin^5(x) - 80 \cdot \sin^3(x) + 20 \cdot \sin(x)] \quad (6.2)$$

$$\sin(3x) = -4 \cdot \sin^3(x) + 3 \cdot \sin(x) \quad (6.3)$$

$$\cos(6x) = -32 \sin^6(x) + 48 \sin^4(x) - 18 \sin^2(x) + 1 \quad (6.4)$$

$$\cos(4x) = 8 \sin^4(x) - 8 \sin^2(x) + 1 \quad (6.5)$$

$$\cos(2x) = -2 \sin^2(x) + 1 \quad (6.6)$$

## 6.2 CIRCUIT DESCRIPTION

Equations 6.1- 6.6 imply that the previously used exponentiating circuit can be utilized to obtain a frequency multiplying circuit. Notice that when the multiplying factor is even, the output appears in the form of a cosine signal. However, it will have the desired frequency. Exponential terms can be obtained by adding more diodes as was done previously in chapter 4. However these terms have to be multiplied by different weights. As can be seen from the above equations, the differences between those weights are large for some outputs while small for others. For the case when large differences exist, one can't use the input dc currents inside each current mirror to synthesize those weights. Another solution is to vary areas of the diodes in the control circuit. For example, to obtain an output with a frequency equal to seven times the input frequency, those areas are selected as shown in Figure.6.1. This results in obtaining the following weights: 0.1, 0.8, 1.6, and  $(6.4 / 7)$  which are proportional to the values in the above equation. Transistors  $Q_{25}$ - $Q_{27}$  and  $Q_{26}$ - $Q_{28}$  have area ratios of 1:10 in order to get a weight of 0.1

for the output of the linear mirror. Next, to get the weight for the squaring mirror,  $Q_{17} - Q_{19}$ ,  $Q_{18} - Q_{20}$  are scaled with 8:1 ratios. This results in:

$$V_{C11} = 2V_T \ln [ I_N / I_S ]$$

$$V_{C21} = 2V_T \ln [ I_N / ( 10 \cdot I_S ) ]$$

$$V_{C13} = V_{C11} + 2V_T \ln [ I_N / I_S ] + 2V_T \ln [ I_N / ( 8 \cdot I_S ) ] = 6V_T \ln [ I_N / ( 8 \cdot I_S ) ]$$

$$V_{C23} = V_{C11} + 2V_T \ln [ I_N / I_S ] + 2V_T \ln [ I_N / ( I_S ) ] = 6V_T \ln [ I_N / ( 10 \cdot I_S ) ]$$

$$V_{C23} - V_{C13} = 6V_T \ln [ I_N / ( 0.8 \cdot I_S ) ] \quad ( 6.7 )$$

Since the gain of the mirror is equal to [see chapter 3]

$$\text{Gain} = \exp [ ( V_{C23} - V_{C13} ) / 2 ] .$$

Then,

$$I_{out} = [ I_N / ( 0.8 \cdot I_S ) ]^3 . \quad ( 6.8 )$$

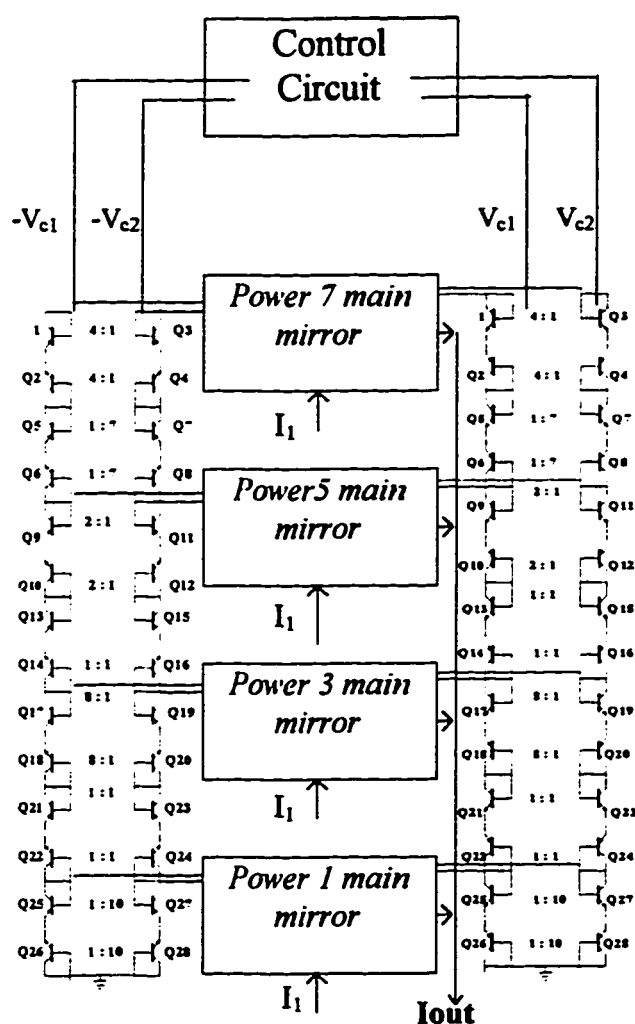
Similarly, to obtain a weight of  $1.6 = 0.1 \cdot 8 \cdot 2$ , transistors  $Q_9 - Q_{11}$  and  $Q_{10} - Q_{12}$  have area ratios of 2:1.

On the other hand, for the case when the output is required to have a frequency four times the input frequency, these weights become: 1 , 8 .0 and 8.0. Thus diodes can be



maintained at the same area while the input currents to the squaring and power 4 mirrors programmed to have the required weight, which is equal to 8 for both of them in this case.

Simulation results for the outputs of frequency tripler, quadripler,  $\times 6$ , and  $\times 7$  circuits together with their frequency spectrums are shown in Figures. 6.2-6.4 respectively. All these circuits were provided additional DC current sources at their outputs to cancel



( A )

For more details about the main , control and power N circuits, see Figure 5.2.

Fig 6.1. Circuit used to obtain frequency multiplication by 7.  $I_1$  and  $I_N$  are inside the control circuit.

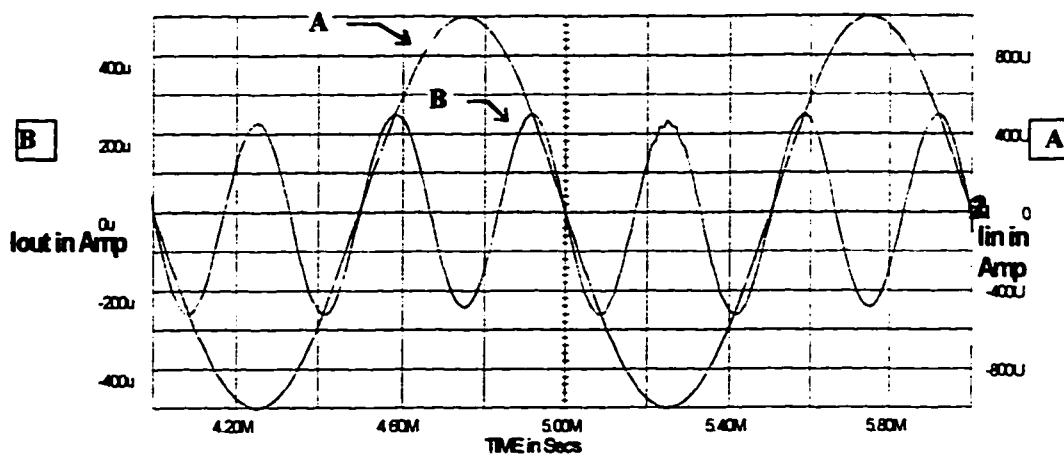


Fig 6.2. a) Input and output currents of a frequency tripler circuit.

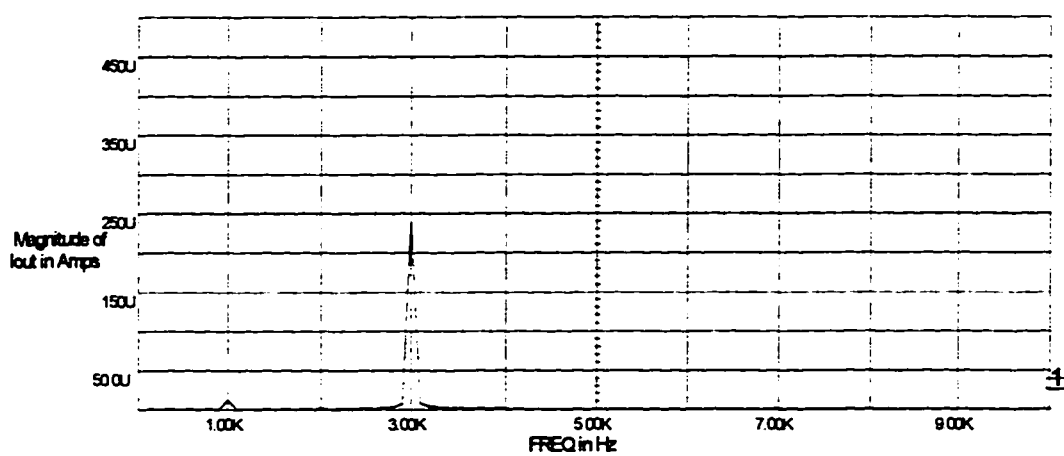


Fig 6.2. b) Amplitude spectrum of output current

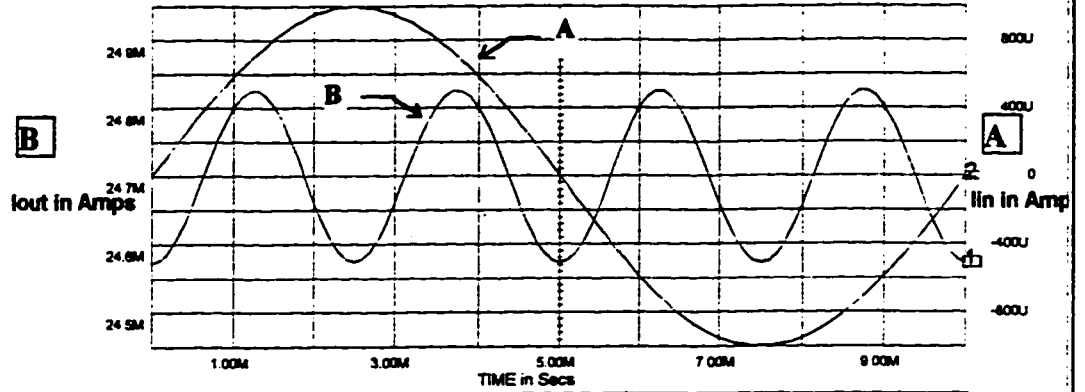


Fig 6.3. a) Input and output currents of a frequency quadrupler

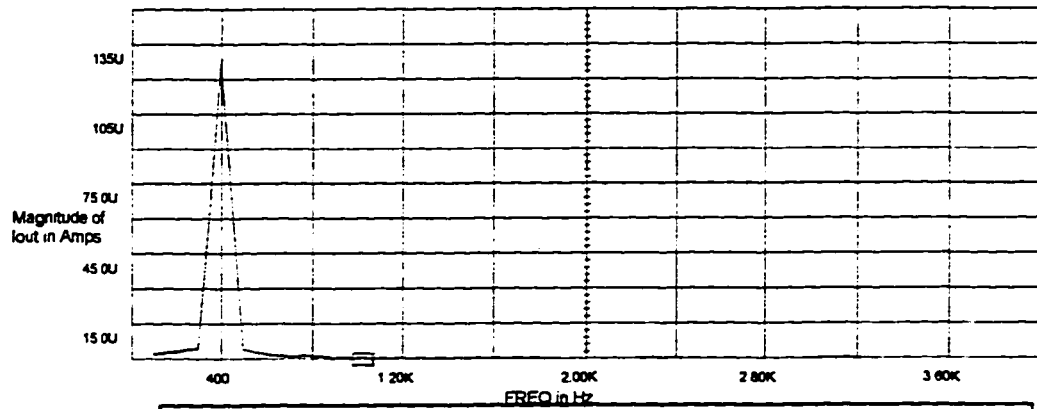


Fig 6.3. b) Amplitude spectrum of output current

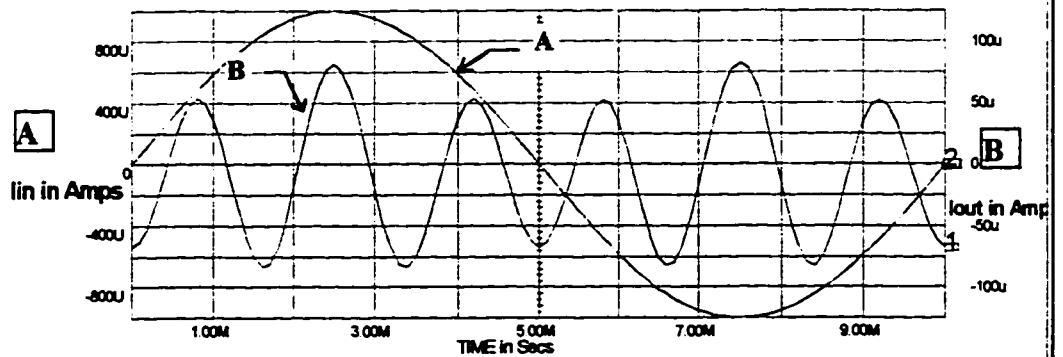
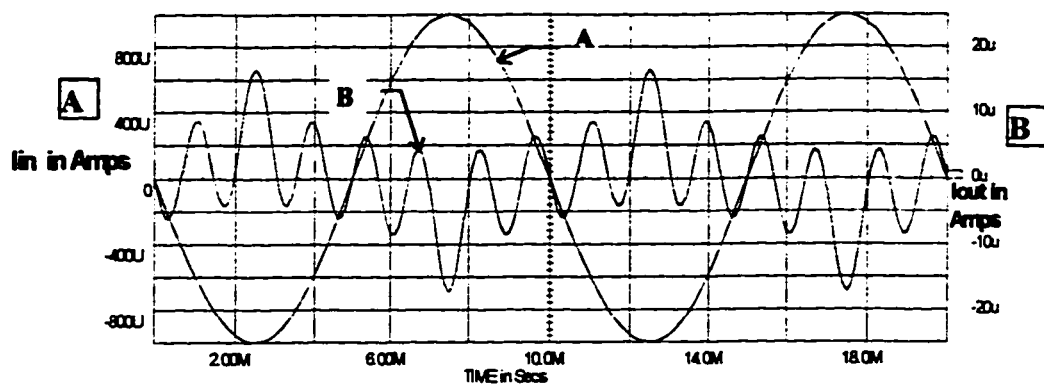
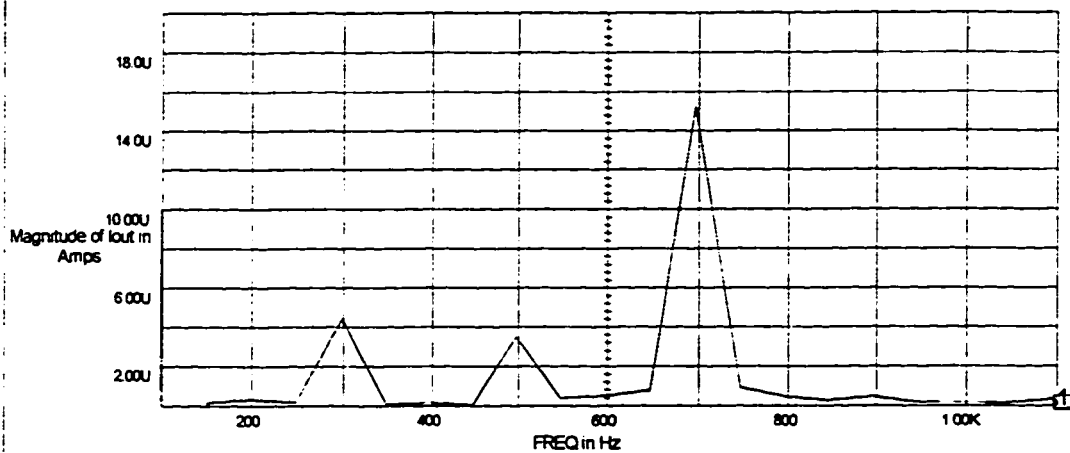


Fig 6.4. a) Input and output currents of a frequency X 6 circuit.



**Fig 6.5. a) Input and output currents of a frequency X 7 circuit.**



**Fig 6.5. b) Amplitude spectrum of output current.**

any D.C offset current that could result because of imbalance between currents generated from positive and negative programmable current mirrors. In all these outputs, as the order of multiplication increases, as the output error increases. This is mainly due to the requirement of high accuracy when the multiplication order is high. However, all mirrors have a nonnegligible error due to the nonzero base currents and to unequal collector emitter voltages. These problems can be reduced if all BJT transistors are replaced with MOS ones operating in the subthreshold region. This will result in a decrease of power consumption too.

This method compares favorably with the method of using a nonlinear device together with a sharp filter. The most commonly used nonlinear device is the diode which, if used, generates a very large number of harmonics other than multiples of the input frequency. Thus a very sharp filter is needed to follow this device if good cancellation of undesired harmonics is wanted. In addition, the filter must contain a capacitive element which is not desirable if the circuit is to be integrated and if the required capacitor is large. Moreover, diodes are well known for their temperature dependence. All these disadvantages are not available in the proposed circuit. However, for simple applications, where small distortion from other unwanted harmonics is not considered severe, this circuit is considered to be large and complicated. This is true, taking into account that the proposed circuit becomes smaller as the required multiplication factor becomes smaller.

The circuit is considered superior than other available methods relying on the use of multipliers to synthesize the previous expressions, see [29] and [30]. These multipliers are much more area consuming than the proposed one. Also, some of them rely on the use of OTA's which are considered to be very temperature dependent. However the circuit can't provide frequency division which has a good number of applications too. This will be the subject of future work.

### **6.3 COMPARISON WITH OTHER CIRCUITS**

The circuit proposed in the preceeding section has a number of advantages over previously published ones. The main advantage is the flexibility provided by the use of PGCMs. By changing few parameters, i.e. current values, the circuit can be programmed to provide frequency multiplication by a different factor. This is a unique feature of this circuit. In addition, the circuit belongs to the class of current mode circuits. This means that it has a good frequency performance. The frequency response of the PGCM, the basic building block of this circuit was shown in chapter two. Also, temperature independence, ability to provide multiple outputs, low input impedance and very high output impedance are other good characteristics.

On the other hand, the circuit fails to provide frequency division of the input signal which is possible in other techniques, see [46, 47]. Also, the circuit is considered to be area consuming when the multiplying factor is small. In order to overcome this problem, PGCMs whose gain is set to zero can be eliminated. However, this results in loss of the programmability feature.

For large multiplying factors, there is a number of techniques that can be used. One of them is to use multipliers in order to implement equations 6.1- 6.6; see [29 ]. Another method is to use a nonlinear element followed by a filter to cancel unwanted frequencies. One last method is to cascade doublers and triplers until the desired output is obtained. All of these methods are generally much more area consuming than the proposed circuit. However, unlike the proposed circuit, these methods can be used to obtain higher multiplying factors.

Accuracy is another issue to be discussed here. As mentioned earlier in this chapter, limitations on the accuracy of the basic PGCM results in reducing the value of the frequency multiplying factor. If the used PGCMs are perfectly accurate, this factor can be increased much more. However, this means that transistors used must have infinite values of  $\beta$  and Early voltage. So, as these values increase as the accuracy enhances specially when the multiplying factor is large. Also, the input signal must be small in order to avoid nonlinearities of the input transistors.

Other frequency multiplying techniques, mentioned previously, have their own sources of errors too. For example using a nonlinear element followed by a filter requires a high order complicated filter in order to obtain high multiplication orders. This could lead to very large circuits, specially when the required accuracy is high. This is not acceptable if the circuit is to be integrated as part of a larger system. Also, the use of multipliers to obtain high order frequency multiplication is not recommended. This is because the required number of multipliers will be extensively large. Also, this reduces the accuracy of the resulting circuit because errors from all multipliers will accumulate. The same thing is true if doublers and triplers are to be used. However, the size of the resulting circuit depends on the subcircuits used. In general, the proposed circuit is smaller in area but not as accurate as the other techniques when the multiplying factor is large.



## CONCLUSION AND FUTURE WORK

In this work, a programmable current mirror was introduced. The circuit was tested and shown to exhibit a good frequency response over a wide bandwidth and a wide range of accurate gain programmability. The usefulness of this circuit in current mode analog signal processing was proved through different linear and nonlinear applications. The major advantage obtained using PGCMs is the flexibility of the resulting circuits due to their electronic programmability. In addition, the ability of these circuits to provide multiple outputs with different linearly or nonlinearly programmable gains was the key of success of their use in the linear and nonlinear applications considered.

One of the most important applications discussed is the electronically programmable analog function synthesizer. This circuit has shown a great flexibility because it can be digitally programmed to synthesize different analog functions that can be expressed using Taylor series. Results obtained by simulation are in very good agreement with theoretically obtained outputs. Also, frequency multipliers were designed based on the basic exponentiating block obtained before. However, frequency multiplication of more than seven times the input frequency was not possible because of the requirement of

highly accurate circuits. This inaccuracy is due to the nonzero value of the base current in BJT transistors.

Other applications include universal filtering, oscillating circuit, multiplication, division, and piecewise linear function approximation. For each application, few modifications to the basic linear PGCM were done to obtain the desired function. The universal filter that was shown, with its great controllability, can be used as a building block to construct a wide variety of more complicated transfer functions. These transfer functions can also be time varying. Similarly, the oscillator circuit that was shown can be easily part of a phase locked loop. The maximum error in linear circuits outputs is not more than 16% while it is less than 5% for other nonlinear applications. This is because of the relatively large number of transistors used to construct linear circuits.

Although all circuits presented in this thesis were built using BJTs only, in future, MOS transistors can be used too. However, these have to be operated in their weak inversion mode in order to utilize the exponential  $I - V$  relationship of their input. The main advantage of using these transistors is the high accuracy that can be obtained due to their negligible gate current. Also, area and power consumption of resulting circuits will be much reduced. However, they are suitable only for relatively low frequency applications. Finally, analog function approximation using mathematical expressions other than the Taylor series will be the subject of future research.

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